ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Chemical Mechanical Planarization

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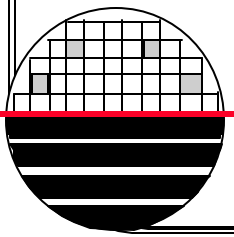
CMP

Chemical Mechanical Planarization

Polishing for the purpose of planarizing integrated circuit structures, and other microelectronic devices.

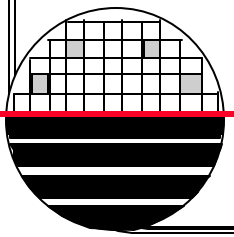
Chemical Mechanical Polishing

Includes traditional polishing, eg. Optics, semiconductor wafer preparation, metals

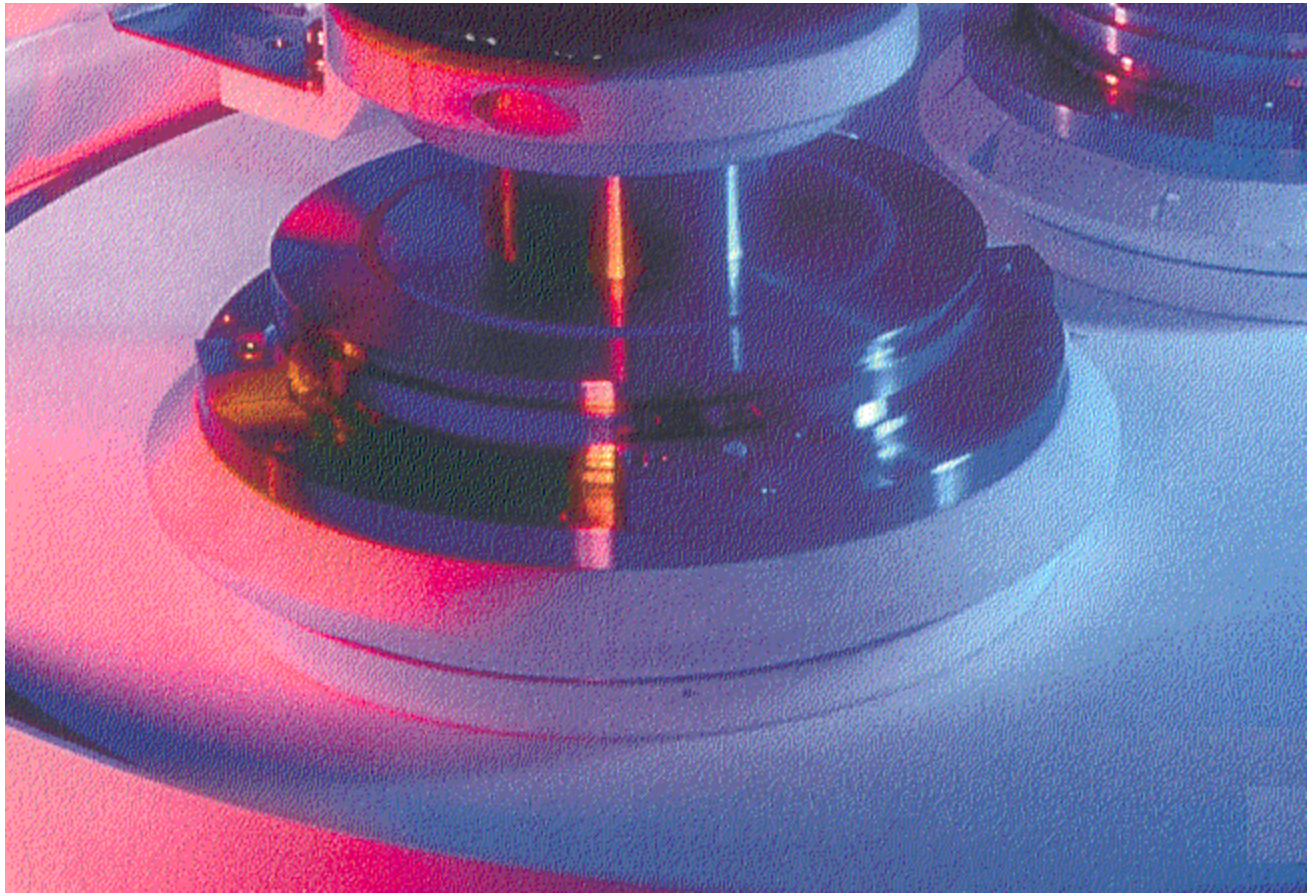


OUTLINE

Introduction
What do we mean “to planarize” an IC?
Why do we need to planarize?
Are there other ways to planarize?
Principles of polishing and planarization
What is CMP of Integrated Circuits?
Why is CMP so great?
Copper Interconnect
References
Homework



CMP

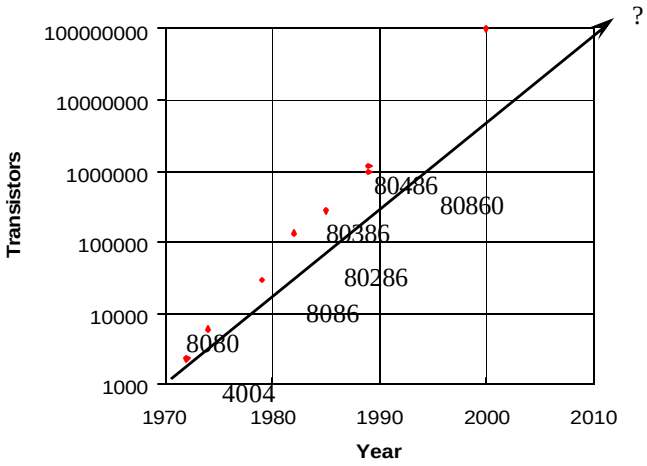


MOORE'S LAW

The number of transistors per chip doubles every 18 months, at no cost to customers.*

The industry has kept pace with Moore's Law:

- Transistors keep getting smaller.
- Transistors keep getting closer together.
- Transistors keep getting faster.



The result of these trends:

Real estate on a chip is very expensive. A chip can no longer be built like a printed circuit board with wires (metal pattern) taking up most of the chip area. The patterned metal layers are placed above the chip and separated by insulators. This is called a multilevel interconnect system.

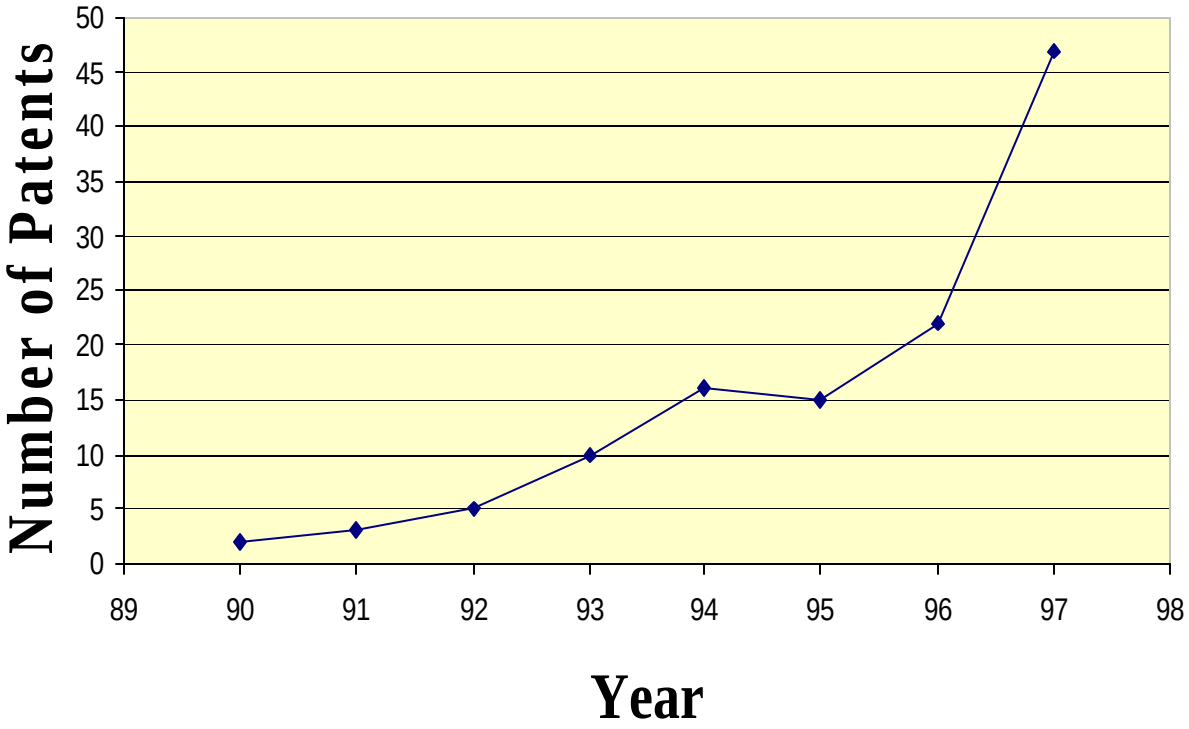
SIA ROADMAP

YEAR / ITEM	1997	1999	2001	2003	2006	2009	2012
CD-GATE	0.25	0.18	0.15	0.13	0.10	0.07	0.05
CD-METAL	0.30	0.22	0.18	0.15	0.11	0.08	0.06
DRAM	256M	1G	2G	4G	16G	64G	256G
Size (mm)	22x22	25x32	25x34	25x36	25x40	25X44	25X52
# MASKS	22	22	23	24	24-26	26-28	28
# METAL LEVELS							
DRAM	2-3	3	3	3	3	3	3
Microprocessor	4-5	5	5-6	6	6-7	7	7-8

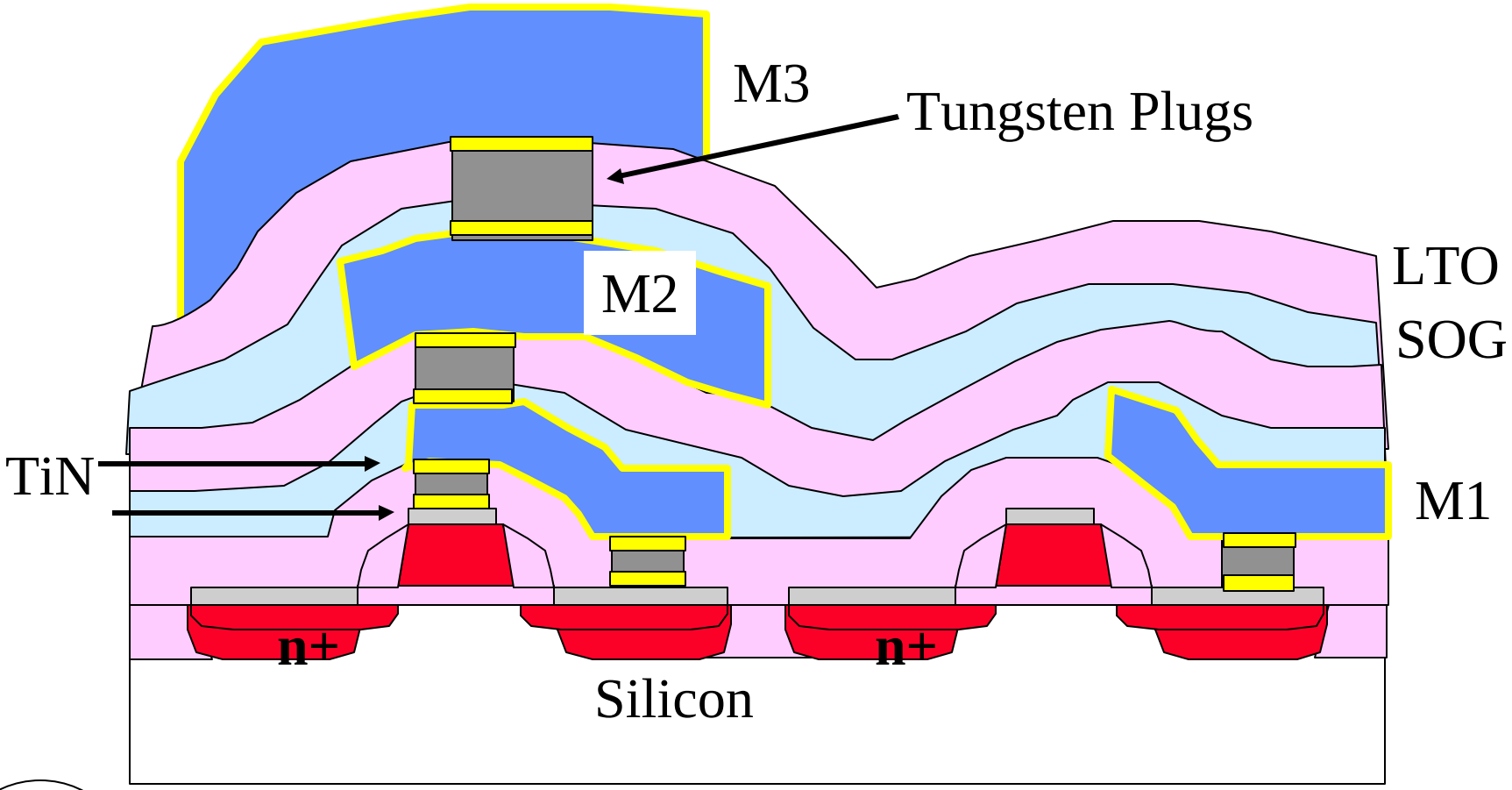
For each additional mask, you add another metal CMP step.

PATENT ACTIVITY ON CMP

US Patents Issued, CMP Area



0.5 μM THREE LEVEL METAL PROCESS NO CMP

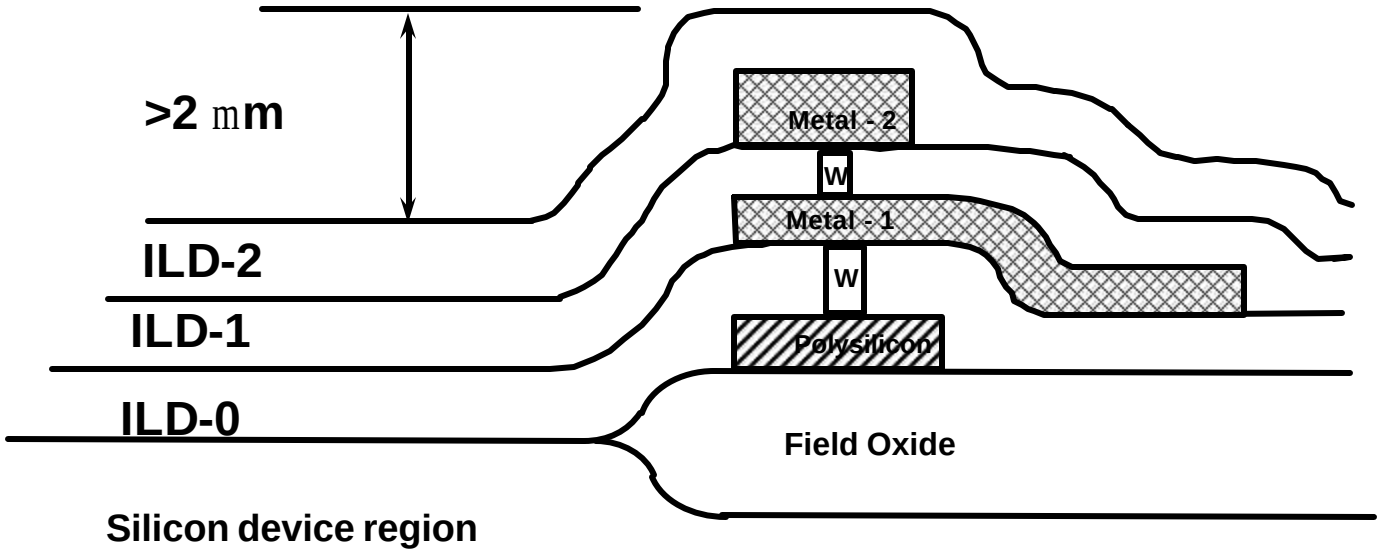


The average number of metal layers on high-end ICs is 4.

Electronic News, July 15, p.1, (1996)

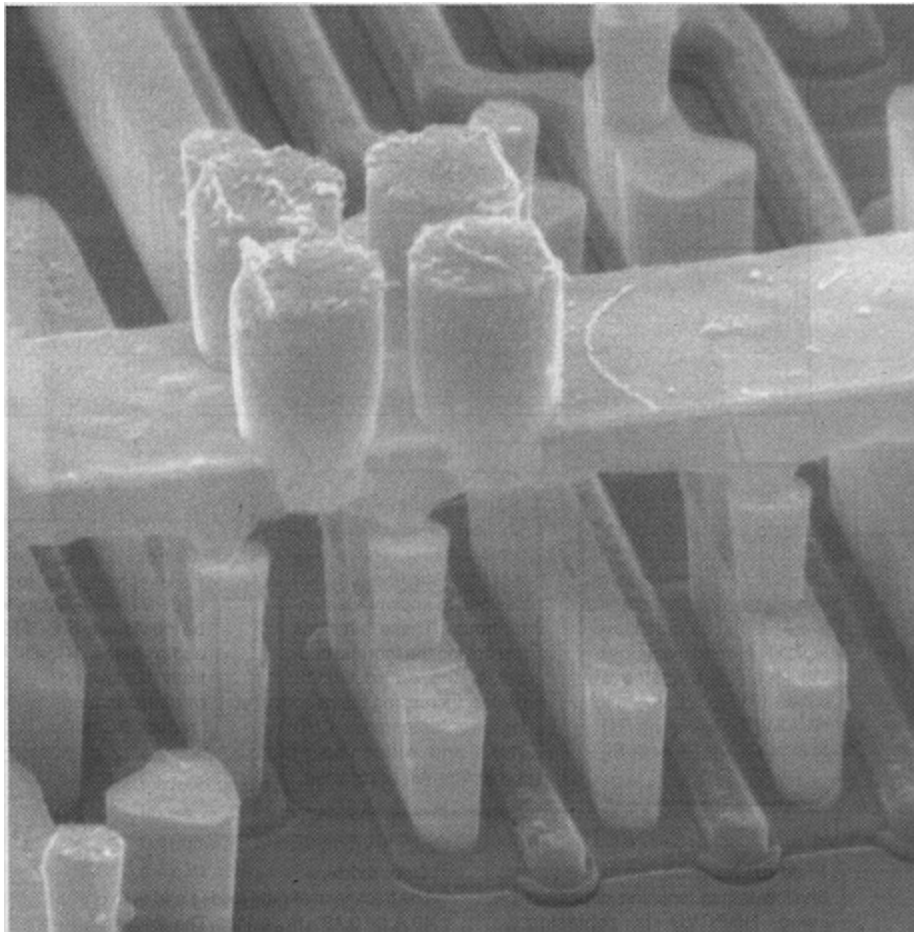
ADDITIVE STEP HEIGHTS WITH UNPLANARIZED MULTILEVEL INTERCONNECTS

§ Multilevel Interconnects required for high-density integrated circuits.
§ Build-up of patterned layers degrades planarity of the surface.
§ This is worse case. Several partial planarization techniques are in common use.



SIX LAYER ALUMINUM, W PLUGS, CMP, DAMASCENE OF LOCAL W INERCONNECT

Six levels aluminum interconnect with tungsten plugs, CMP, and damascene of local tungsten interconnect for 0.18 µm gates.

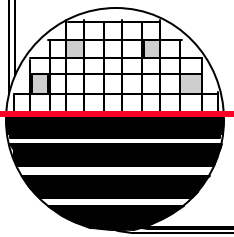


WHAT TO WE MEAN, TO "PLANARIZE AN INTEGRATED CIRCUIT"?

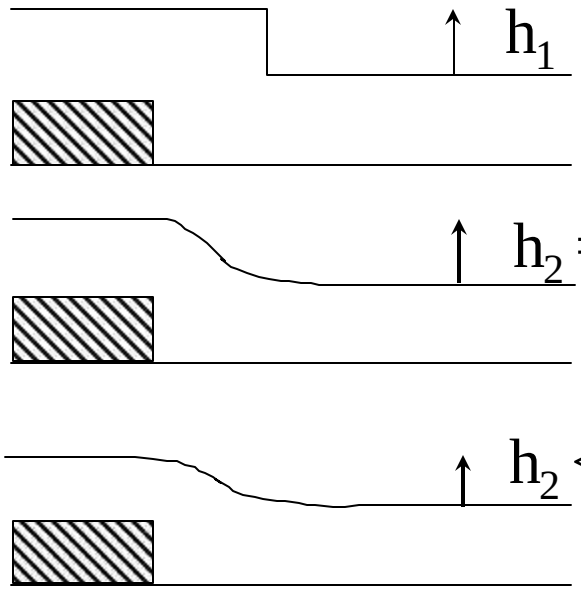
Planarization is one or both of the following :

a. Topography smoothing:
the conversion of abrupt, vertical steps to gradually sloping transitions.

b. Step height reduction:
the reduction of elevation differences



SMOOTHING VS. STEP HEIGHT REDUCTION



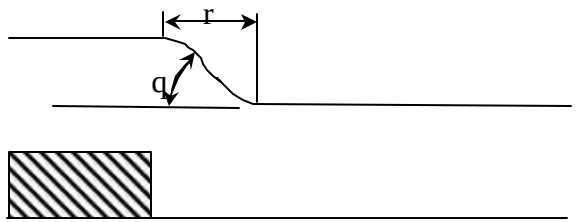
Unplanarized Step

Smoothing, no step height reduction.

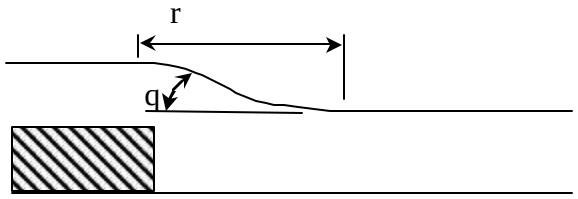
Smoothing, with step height reduction.

$$\textbf{Degree of Planarization} = 1 - \frac{h_2}{h_1}$$

PLANARIZATION RANGE



Short Range: r =1-2 μm
θ = 30 - 45 deg.



Long Range: r = 100 - 200 μm
θ = 1- 0.01 deg.

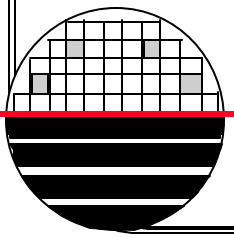
Global Planarization

$$\textbf{Planarization Range (r)} = \frac{\textbf{Post-Step Height}}{\textbf{tan (q)}}$$

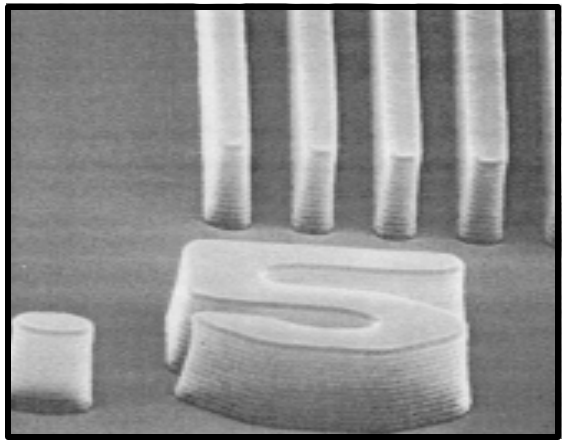
WHY DO WE NEED TO PLANARIZE?

§ **High density circuits**

- **Sub-micron features require the highest resolution imaging techniques. This implies short wavelength and high numerical aperture lenses resulting in small depth of focus. CMP provides a flat surface so small depth of focus is not an issue.**
- **Sub-micron devices require shallow trench isolation which requires CMP**
- **Sub-micron devices at high packing density require more than three levels of sub-micron interconnect wiring which requires CMP.**



CANON FPA-2000 i1 STEPPER



i-Line Stepper $\lambda = 365$ nm

NA = 0.52, $\sigma = 0.6$

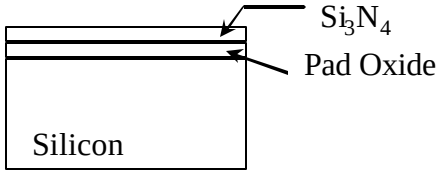
Resolution = $0.7\ \lambda$ / NA = ~0.5 µm

20 x 20 mm Field Size

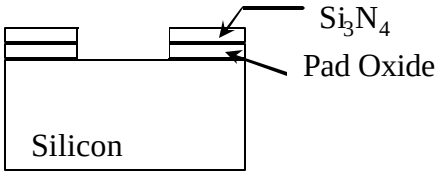
Depth of Focus = $k_2\ \lambda/(NA)^2$

= 0.8 µm

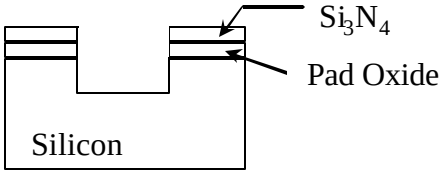
SHALLOW TRENCH ISOLATION (FEOL)



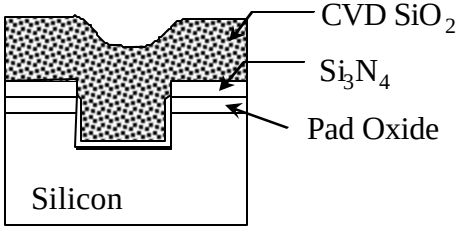
1. Thermal Oxidation Deposit Nitride



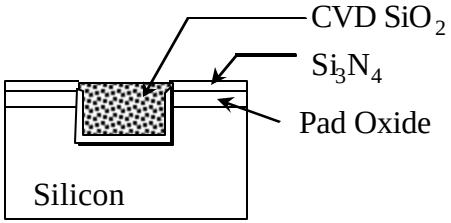
2. Pattern and etch Nitride and oxide



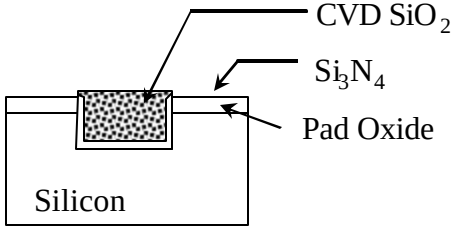
3. Etch trench in silicon substrate



4. Thermal Oxidation Deposit CVD Oxide



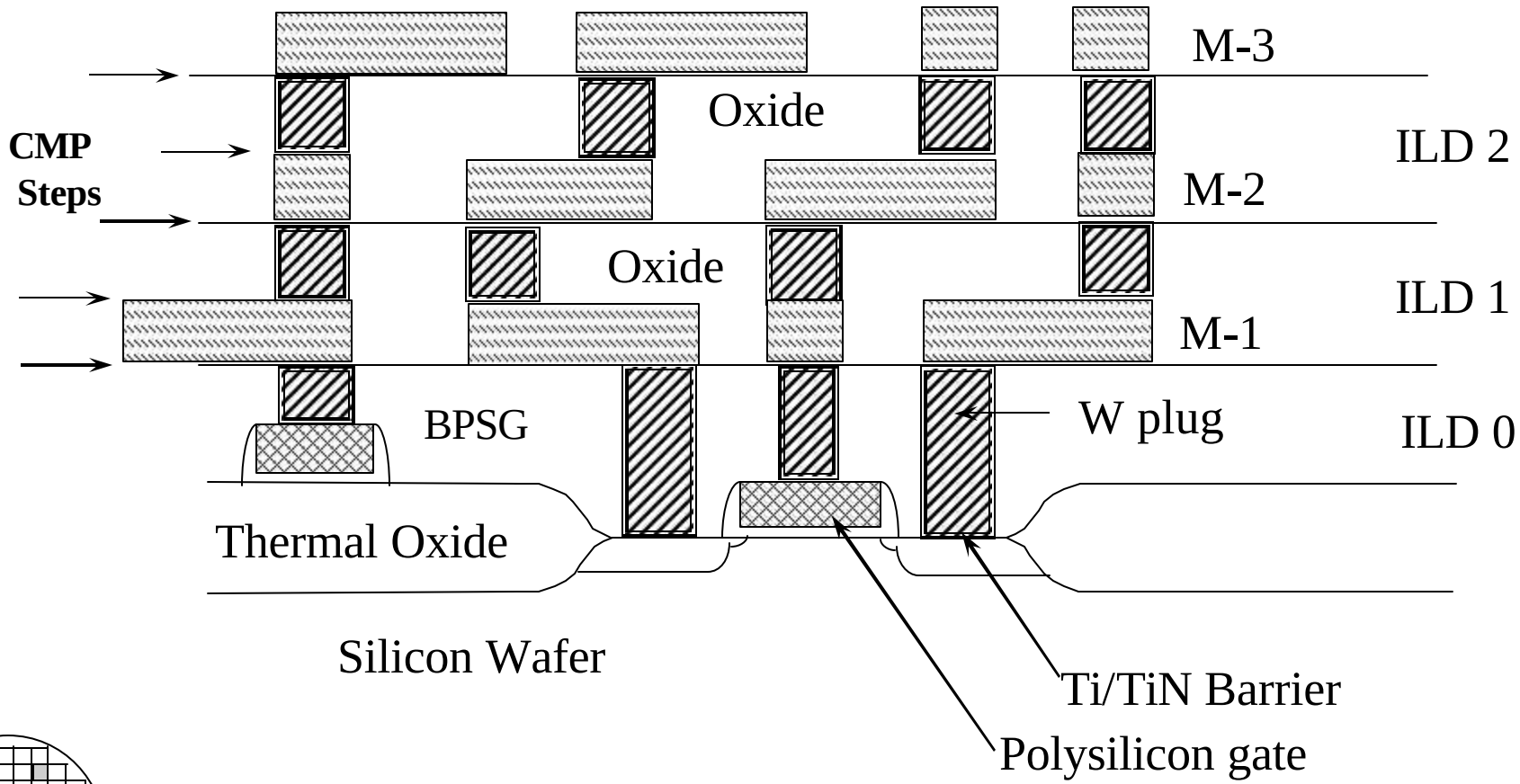
5. CMP of oxide to Nitride polish stop



6. Chemical strip of Nitride

Nitride polish stop and its subsequent removal helps to minimize dishing in trenches.

CROSS SECTION OF MULTI LAYER METAL STRUCTURE PLANARIZED BY CMP



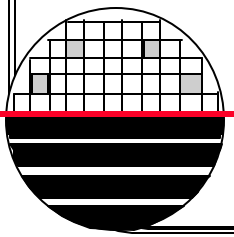
WHAT IS PLANARIZED, SPECIFICALLY?

- **Front end Applications (FEOL) -** Devices in the active regions of the silicon wafer, such as:
  - **Shallow trench isolation (STI)**
  - **Trench capacitors**
  - **Inter-polysilicon dielectrics**
- **Back end applications (BEOL) -** Metal and dielectric films which comprise the wiring of the millions of devices in the silicon wafer.
  - **Pre-metal dielectrics (doped oxides, e.g.BPSG, PSG)**
  - **Lateral and Vertical interconnections (Al, W, Cu, Ta, Ti, TiN, doped Silicon Cu-alloys, Al-alloys)**
  - **Intermetal dielectrics (TEOS, SOG, SiO_2, BPSG, PSG, Si_3N_4)**
  - **Polymers (Polyimide)**

METHODS OF PLANARIZATION

- **Thermal flow**
- **CVD and Reflow**
- **RIE Etchback of sacrificial layer**
- **Spin-on-glass (SOG)**
- **Variations of above**

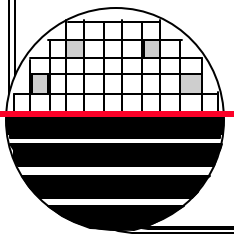
- **CMP**



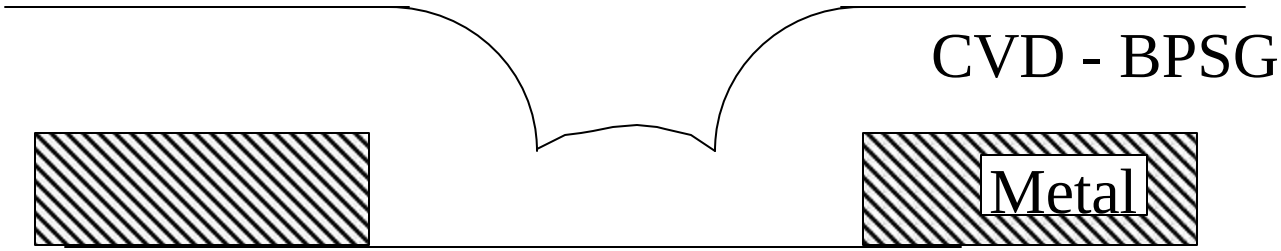
WHY IS CMP SO GREAT?

- **It is the only process which can planarize on a global scale.**
  - **Alternative planarization processes are affected by the pattern size and density.**

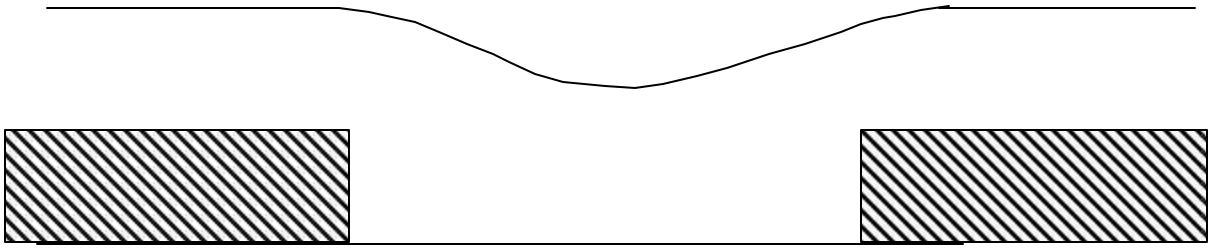
- **It is an <u>enabling</u> process:**
  - **Maximizes lithographic performance.**
  - **Improves cleaning.**
  - **Reduces yield limiting defects from other processes.**
  - **Permits the use of difficult-to-etch metals such as Cu.**



THERMAL FLOW OF BOROPHOSPHOSILICATE GLASS

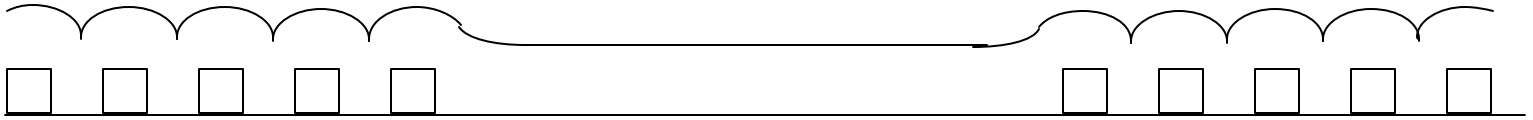


As-deposited



After thermal flow

PLANARIZATION BY REFLOW OF DOPED GLASS*

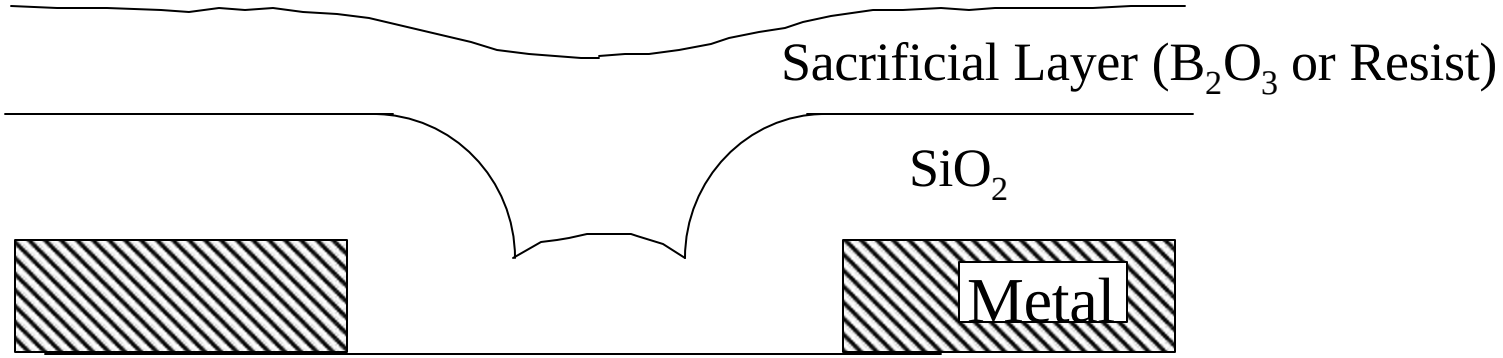


After deposition of doped glass by CVD

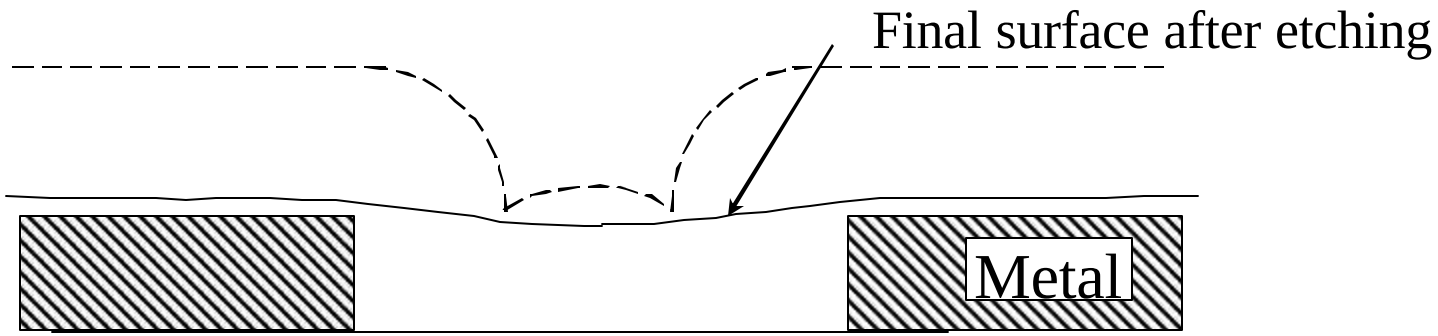
Local planarization after reflow of doped glass
reflow does not provide global planarization.

*PSG, BPSG, or BSG

FLOW AND SACRIFICIAL ETCHBACK

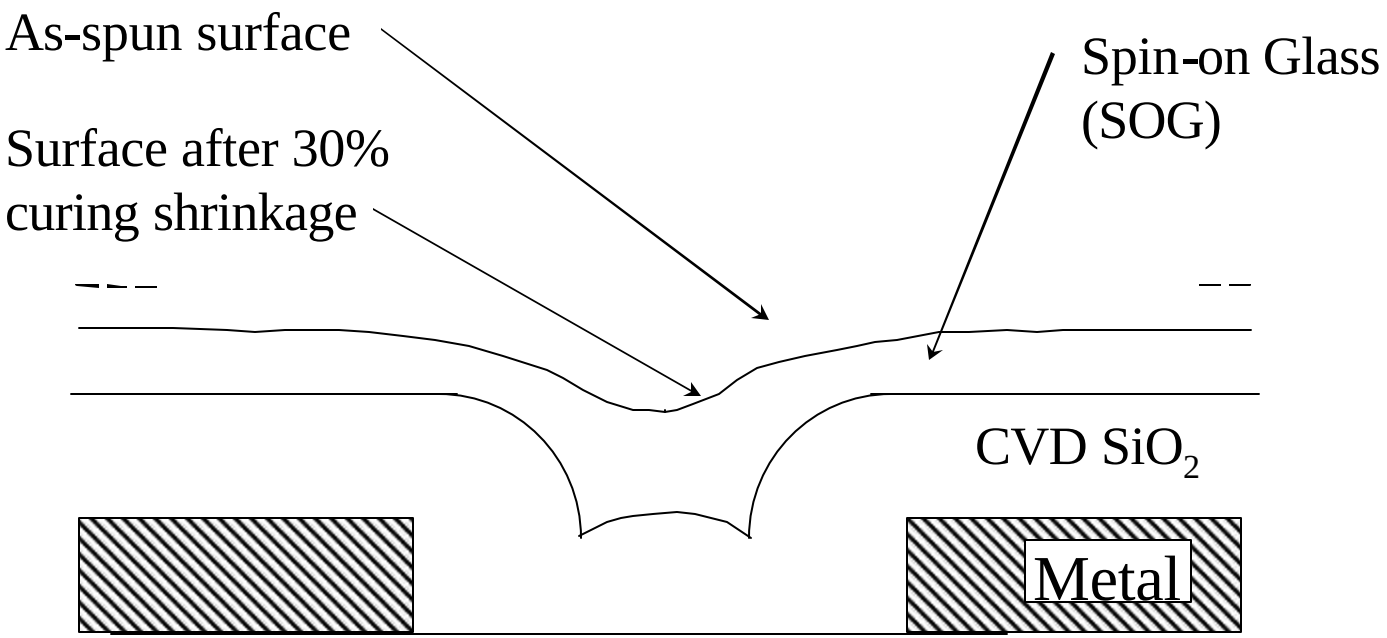


Thermally flowed B_2O_3 or as-deposited photoresist applied as a sacrificial layer to be etched by RIE



Planarized surface after RIE etchback

NON-SACRIFICAL PLANARIZING LAYERS

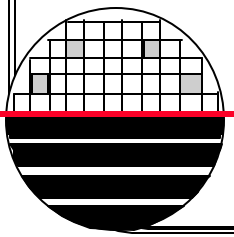


SOG does not provide global planarization

WHAT IS CHEMICAL MECHANICAL PLANARIZATION?

§ **CMP**

- **To flatten the surface of an integrated circuit by using a polishing process, i.e., by rubbing with a pad and slurry to remove the high regions of the circuit.**
- **High regions on the circuit should be removed by an equal amount, regardless of their area. Removal should be uniform across the whole wafer (many circuits).**
- **Removal must occur without causing damage to the circuit, or the wafer.**



WHAT IS LAPPING and POLISHING?

Lapping –

To planarize or to create desired shape or dimension.

To produce a uniformly abraded surface with known degree of sub-surface damage (~1/4 of grit size)

Slurry of water and 8-micrometer alumina grit.

Cast iron lapping plates, double side lapping produces flatness and parallelism < 2 µm.

Typical removal, 50 µm per side.

Polishing –

To remove residual damage from lapping

To produce no new damage

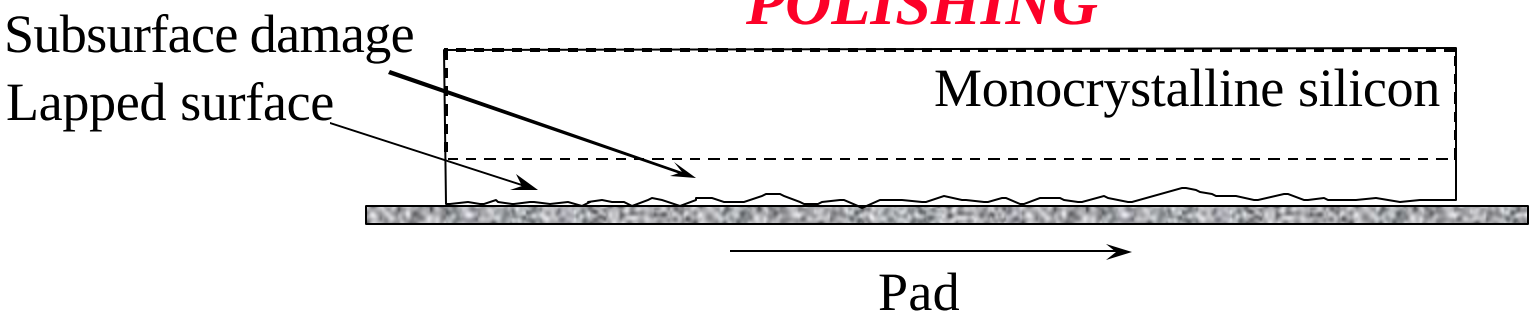
To create a microscopically smooth surface

Does not change the shape of the surface

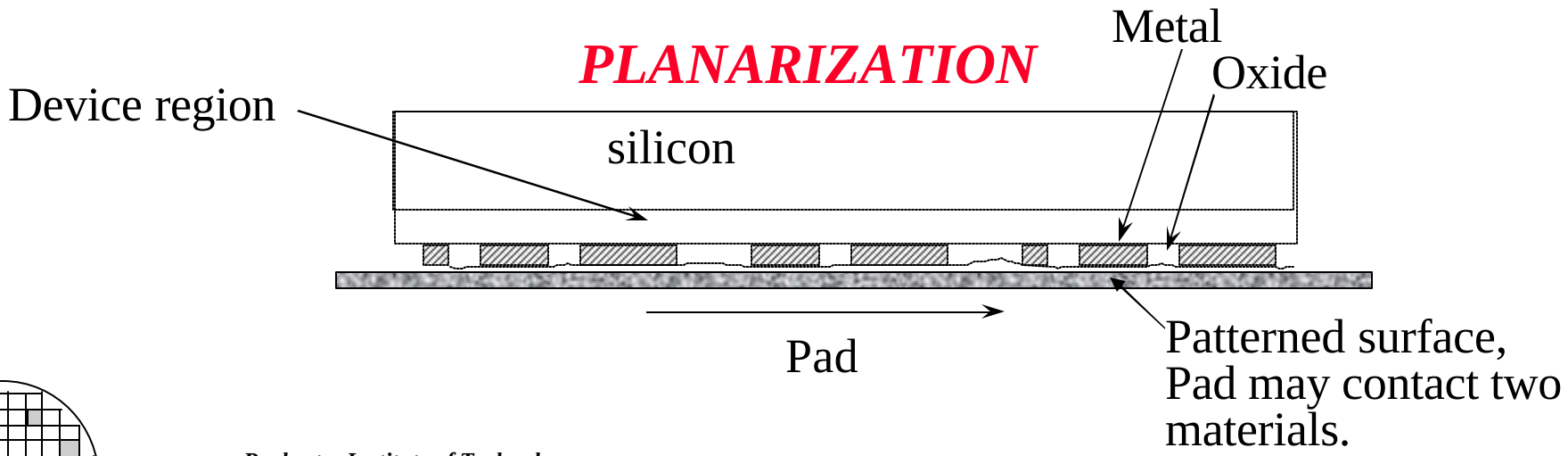
Gentle rubbing with a soft pad saturated with polishing slurry (CeO_2, Fe_2O_3, ZrO_2, SiO_2). It involves both a chemical and a mechanical component. At pH=10.5

SILICON POLISHING VS IC PLANARIZATION

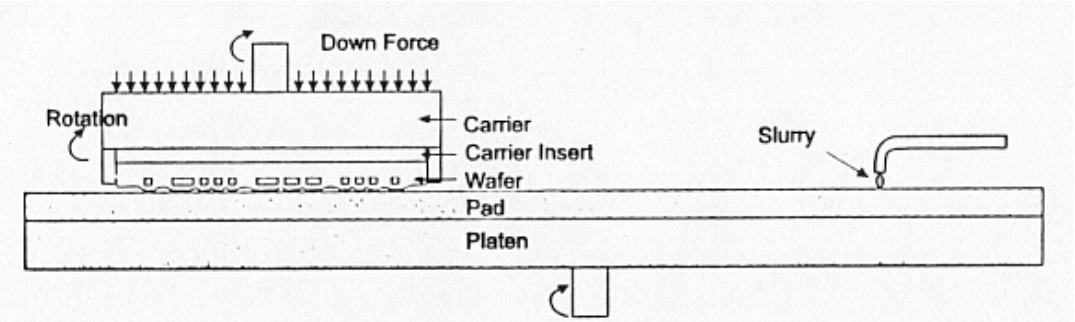
POLISHING



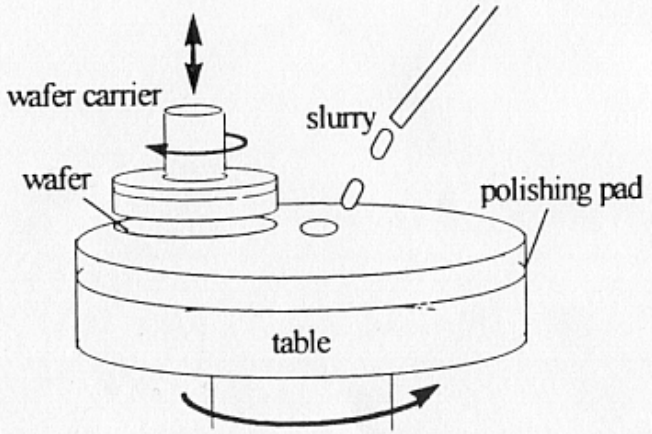
PLANARIZATION



CMP EQUIPMENT SCHEMATIC CONVENTIONAL ORBITAL

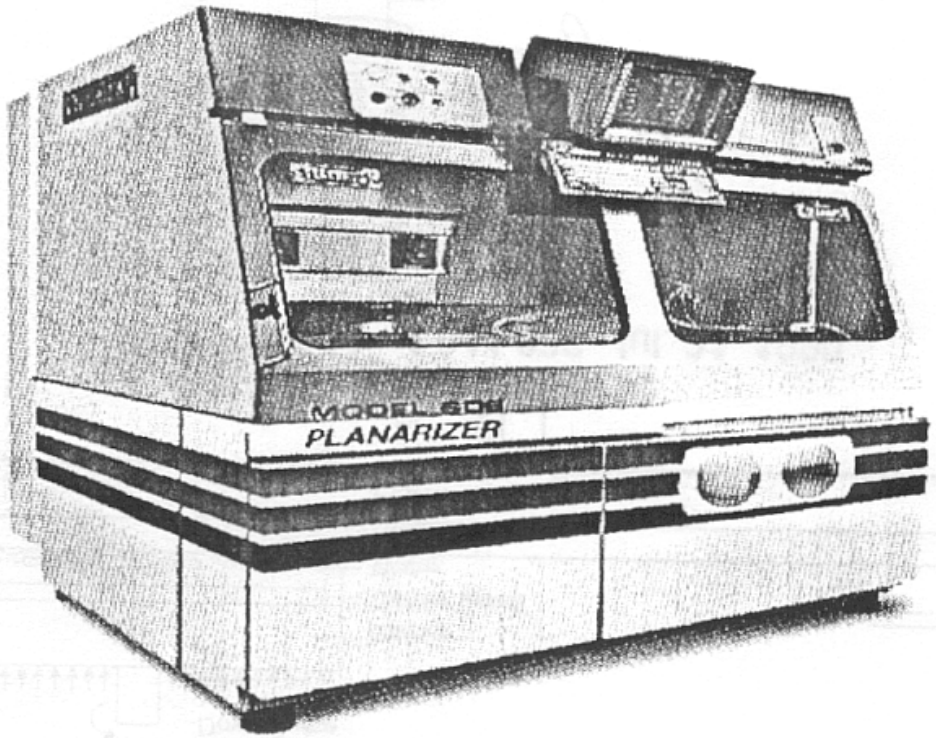


IBM Patent: 4,944,836, Jul. 31, 1990



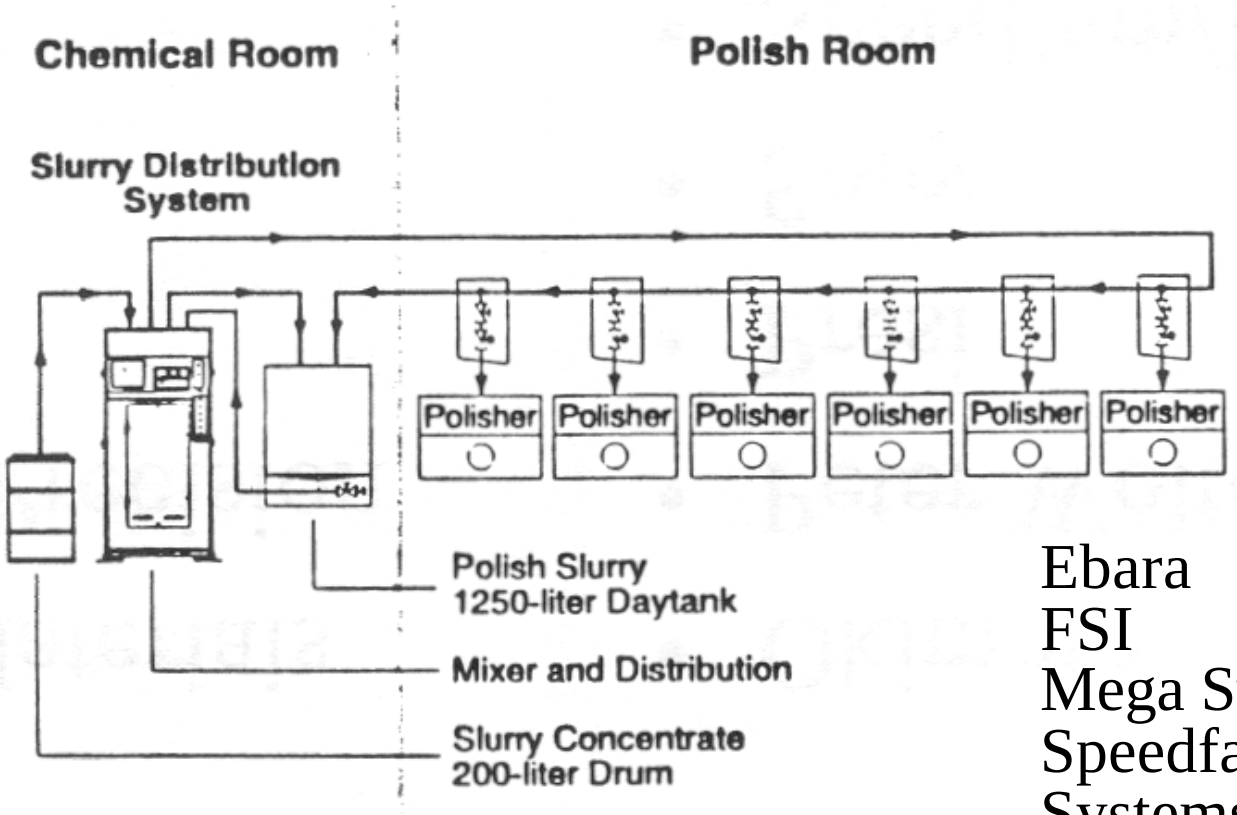
WESTECH

CMP TOOL MANUFACTURERS



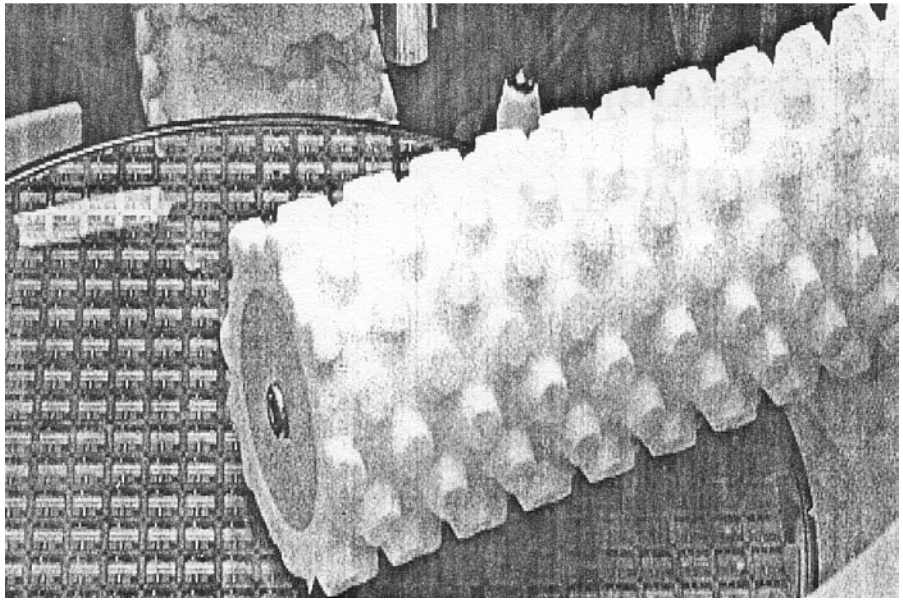
Applied Materials
Cranfield Precision
Ebara
Fujikoshi
Lapmaster
Mitsubishi
Nutool
Okimoto
Peter Wolters
Presi
Sony
Speedfam/IPEC
Strasbaugh
Toshiba

SLURRY DISTRIBUTION SYSTEMS



Ebara
FSI
Mega Systems
Speedfam/IPEC
Systems Chemistry
Universal Photronics

POST CMP CLEAN TOOLS



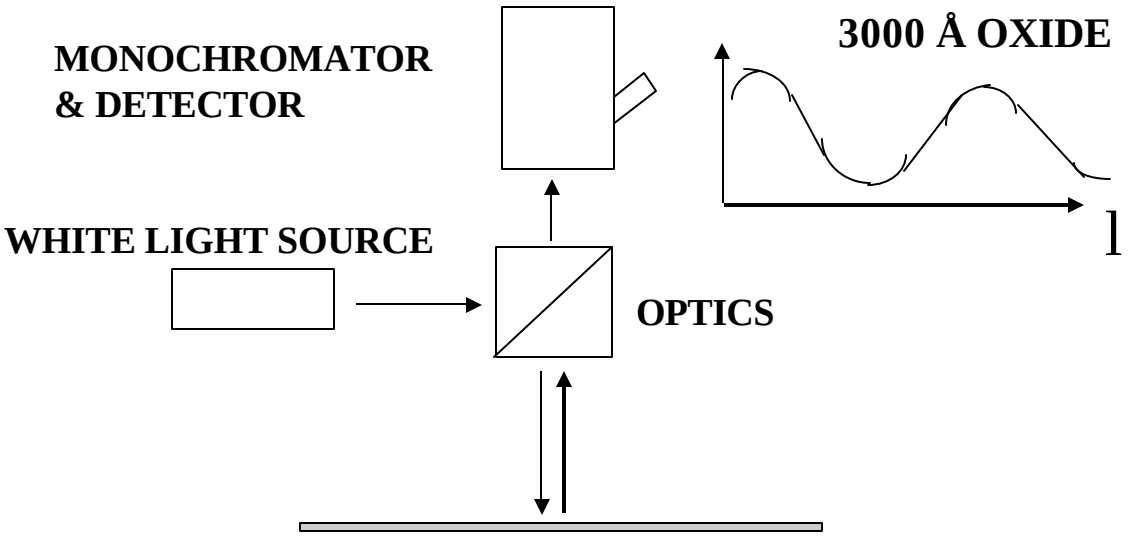
Tools

- Dai Mippon Screen (DNS)
- Oliver Design
- OnTrak Systems (Lamb)
- Solid State Equipment
- Speedfam/IPEC
- Sumitomo Metals
- Toshiba

PVA Brush Rollers

- Cupps Industrial
- Kanebo
- Merocel
- Syntax
- Universal Photronics

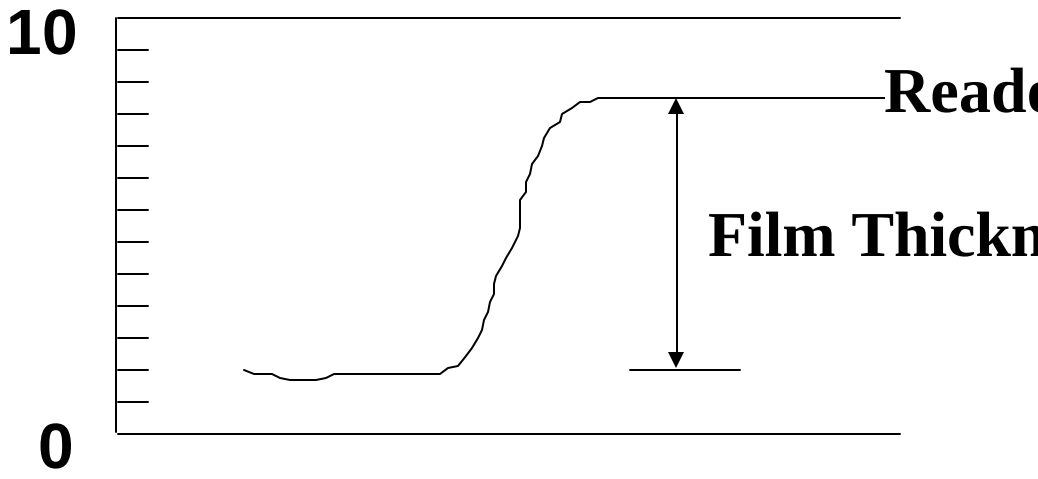
METROLOGY TOOLS



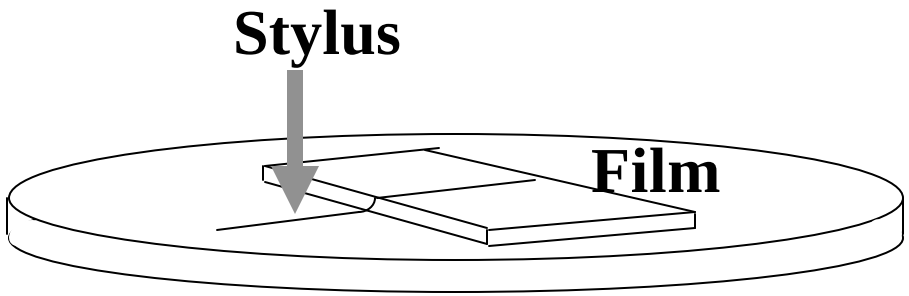
ADE
Bio-Rad
Mamamatsu
Hitachi
Horiba
KLA/Tencor
Matec
Nanometrics
Rudolph Instruments
Speedfam/IPEC
Topcon

Roches
Microe

SURFACE PROFILOMETER



1,000 Å < Max < 1,000,000 Å

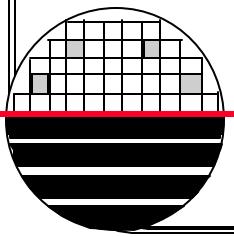


PADS

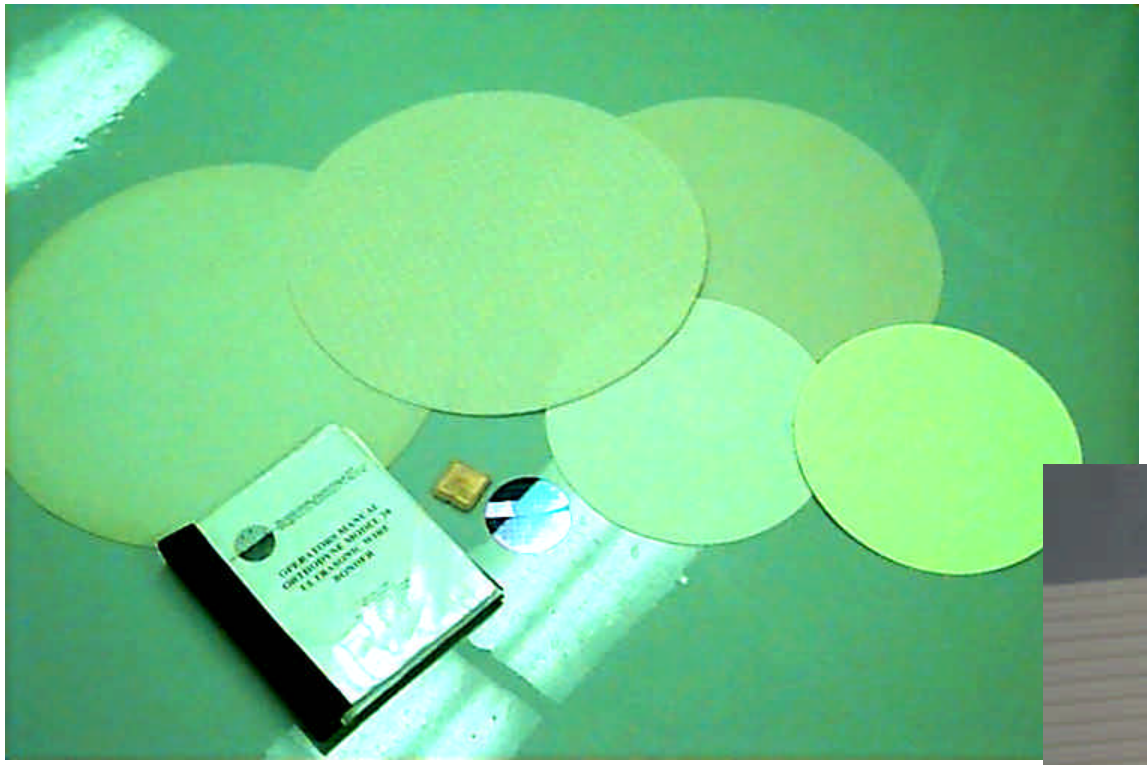
Impregnated – non woven polyester base, saturated with polyurethane which binds the base together when cured. Pad is abrasively buffed to condition it for use. Range of hardness and densities are available.

Cast – foamed polyurethane is cast in molds and cross-linked, after which it is sliced into sheets from 0.020 to 1.25 inches thickness. A wide range of density and hardness is available.

Coated – a non woven polyester base is coated with a polyurethante formulation which forms a skin layer which is abrasively buffed before use. Often used as a final cosmetic polish after stock removal with cast or impregnated pads.

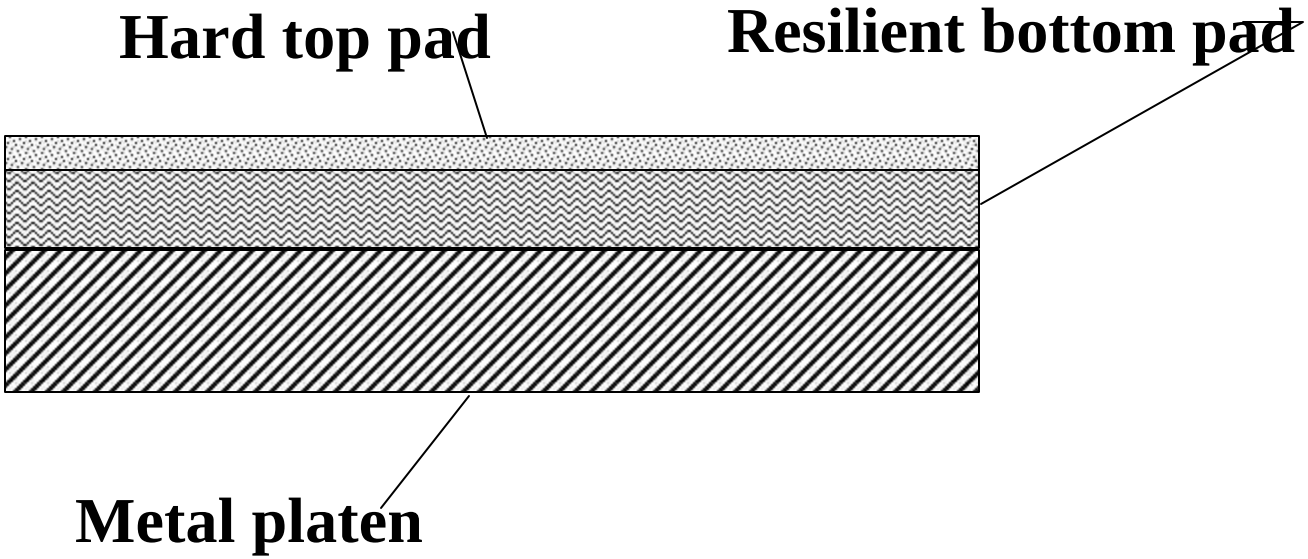


PADS



3M
Cabot
Freudenberg
Fujibo
Kanebo
Rodel
Teijin Mills
Universal Photonics

STACKED PAD



Hard upper pad reduces dishing while compressible lower pad conforms globally to the wafer surface, improving uniformity.

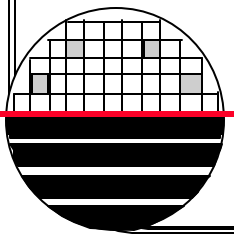
PAD CONDITIONING

Purpose

- to help maintain stability of removal rate in CMP
- To maintain long pad life
- To maintain removal rate uniformity within wafer
- Removes imbedded and caked debris in pad surface
- Exposes uniform pad material
- Abrades pad surface
- Maintains planar pad surface

Technique

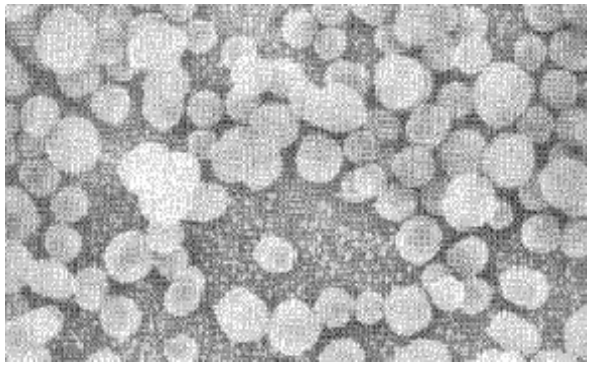
- A diamond plated disc is applied to the pad using a prescribed downward force and rotation program, in the presence of water



SLURRIES

Metals
Colloidal alumina and ferric nitrate, low pH

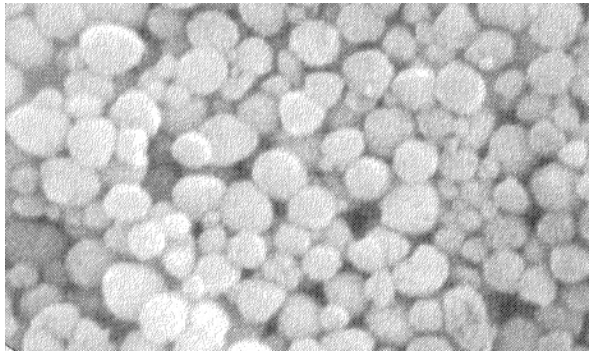
Weak oxide film is formed using MnO2 based polishing agent, which is removed with MnO2 mechanical action.



Oxides
Colloidal Silica (sub micron particle size) in water with KOH or NH4OH, pH of 10.5

Cerium Oxide CeO2 (sub micron particle size), High Ph

Zirconium oxide

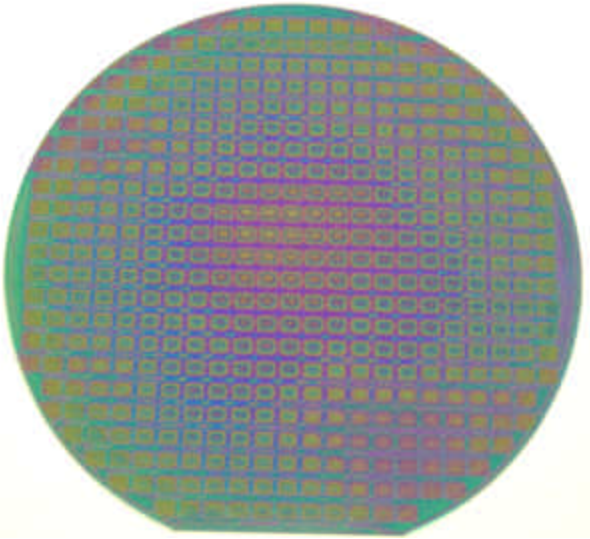


SLURRY MANUFACTURERS

Cabot
EKC Technologies
Fujimi
Intersurface Dynamics
Praxair
Rodel
Transelco/Ferro
Universal Photonics

FACTORY STI PROCESS (FACTSTI)

- Carrier speed: 30 RPM
- Platen speed: 100 RPM
- Without back pressure
- 8 PSI down force (36 PSI on the gauge)
- Slurry (made for STI, see pages below)
- Slurry flow rate (60 mL/min)
- Pad conditioning: before every run
- Temperature: 80°C
- Polishing time: 2min 30 sec for 6500A oxide



After 2.25 minutes of Polishing
Clear almost every die
Even edge die
(Depends on Pattern Density)

CMP SLURRY

Eminess Technologies, Inc.
1620 West fountainhead Pkwy, Suite 510
Tempe, AZ 85282
Tel (408)505-3409, 888-899-1942,
fax (480)951-3842

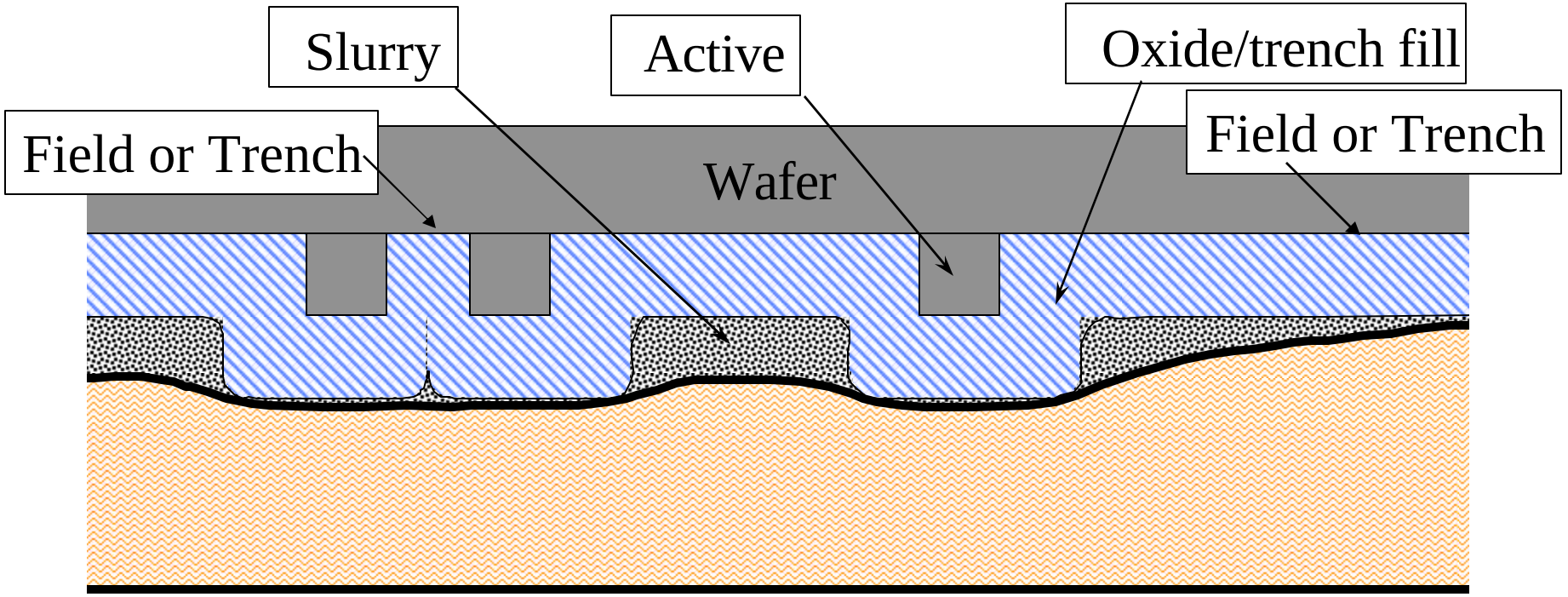
http://www.EMINESS.com
http://www.electronicmaterials.rohmhaas.com

1/05/06 Order:
N-2350-P Nalco 2350, 5 gal pail $166 each, Mfg by Rohm and Haas,
Silica, 70-100nm particle size, weight % 28, KOH, pH 11.4-12.4

R-10027556 Klebosol 1501-50 Colloidal Silica 5 gal pail $255 each,
Mfg AZ Electronic Materials, Clariant's Klebosol line of silica slurrys,50nm particles, KOH pH 10.9 50% solids

R-10087555 EXP CELEXIS CX94S Single Component Slurry, 20Liter pail $235 each, Mfg by Rohm and Haas Ceria 20nm particles, STI, pH ~7

PAD - SLURRY - SURFACE INTERACTION



Pad saturated with slurry.
Polishing pressure greatest on small, elevated features (active).
Pad may contact larger low areas (large field regions) called dishing.

PRESTON'S EQUATION

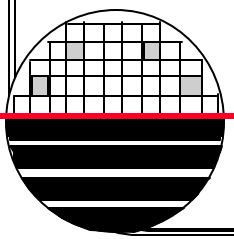
Removal rate is proportional to pressure and velocity:

$R \alpha S F/A$ Or: $\boxed{R = Kp S F/A}$

in which:
R = removal rate
S = relative velocity
F = Force on work piece
A = area in contact with pad.
Kp = Preston coefficient

Volume removal: $RA = Kp S F$

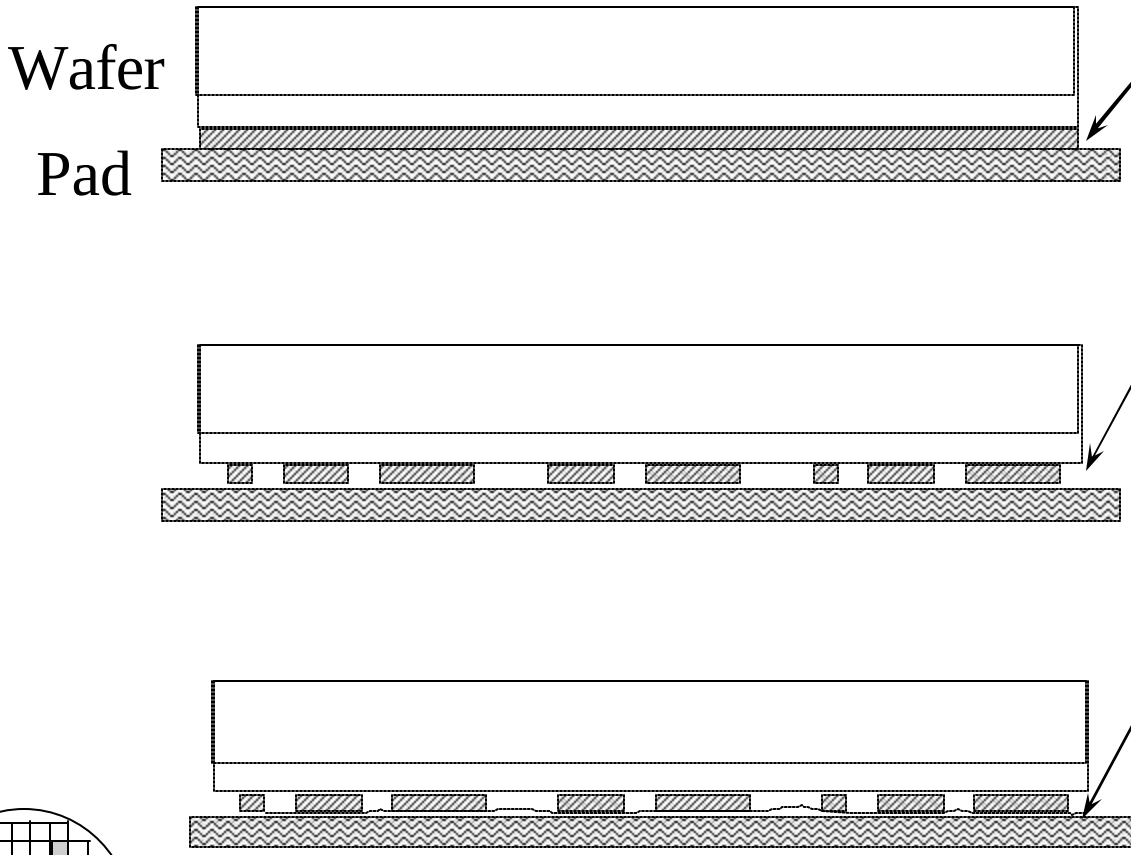
Many polishing processes obey this relationship fairly well, however it ignores any chemical effects.



Preston, F., (1927)

POLISH RATE VS. PATTERN DENSITY

Volumetric rate: RA = Kp F S



Blanket Polishing

Area = Wafer area

Patterned polishing.
No pad contact between features

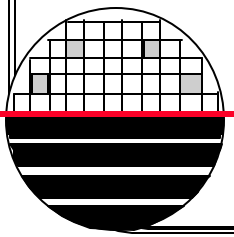
Area = pattern area

Patterned polishing.
Some pad contact between features.

Area = ?

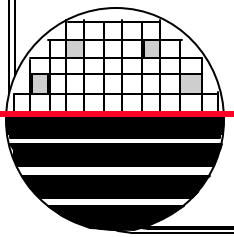
PARAMETERS THAT AFFECT REMOVAL RATE

- Slurry Chemicals
  - pH
  - Buffering agents
  - oxidizers
  - complexing agents
  - concentration
  - dielectric constant
- Slurry Abrasive
  - type
  - size
  - concentration
  - pH
  - suspension stability
- Slurry Flow Rate
- Films being Polished
- Temperature
  - (5X removal rate/ 20 °C)
- Downward Pressure
- Platen Speed
- Carrier Speed
- Pattern Geometries
  - Feature Size
  - Pattern Density
- Pad Type
  - fiber structure
  - pore size
  - hardness
  - elastic and shear modulus
  - thickness
  - embossing or perforations
  - conditioning
  - aging effects
  - chemical durability
- Wafer size

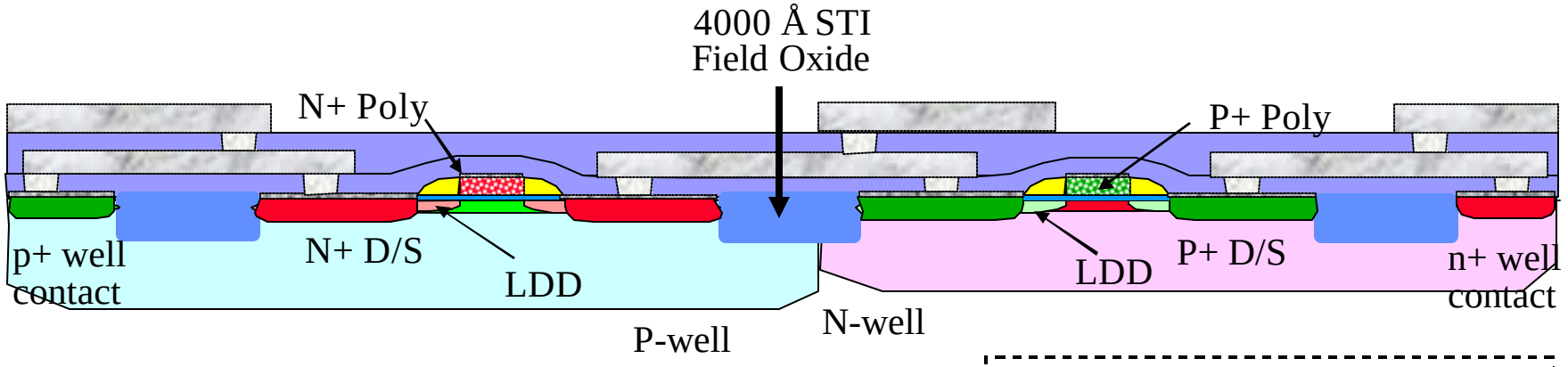


CHANGE AND EFFECT

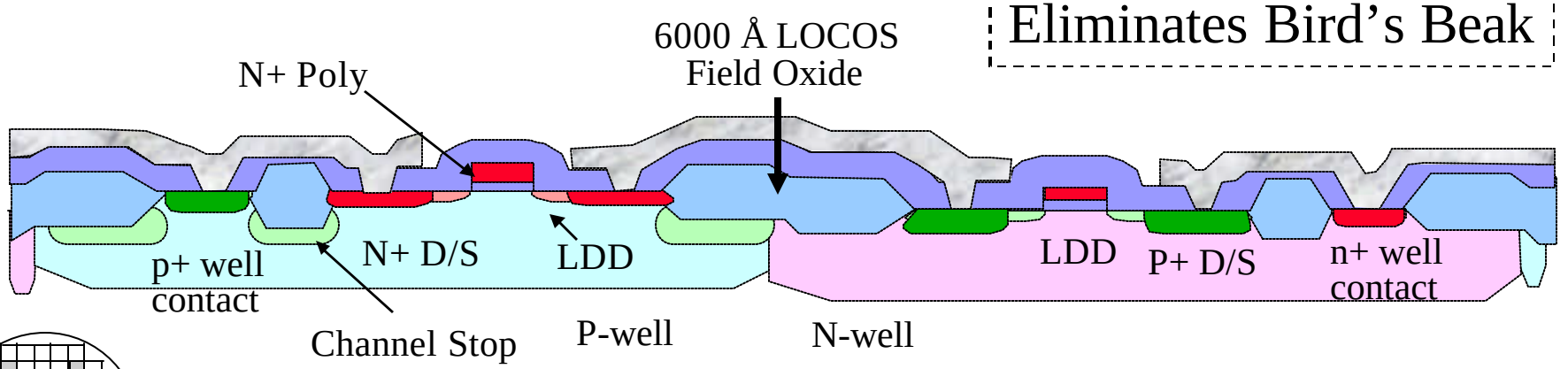
Increase pressure – increase removal rate, degrade surface finish
Increase carrier speed – increase removal rate, degrade uniformity
Increase platen speed – increase removal rate, degrade uniformity
Increase slurry flow – decrease removal rate, improve surface finish



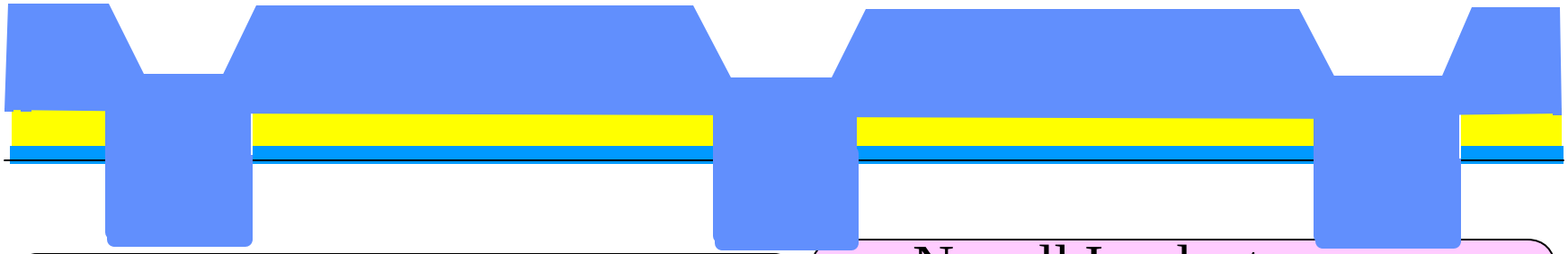
SHALLOW TRENCH ISOLATION (STI)



STI reduces topology
Eliminates Bird's Beak



AFTER LTO TRENCH FILL PRIOR TO CMP

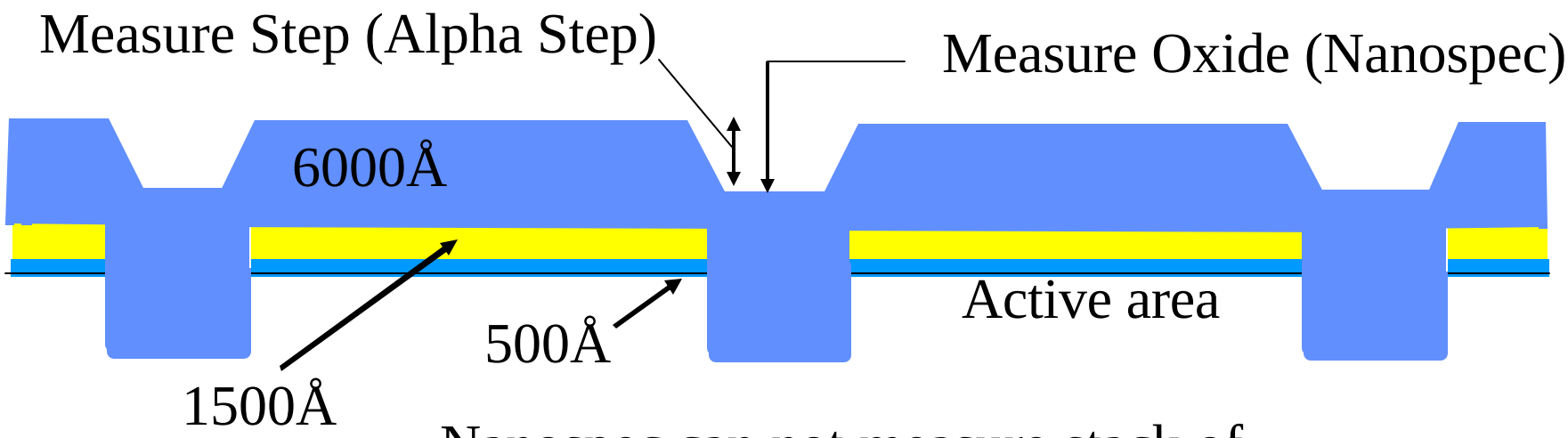


Substrate 10 ohm-cm

Fill 4000 Å trench with
Deposit 6000 Å TEOS

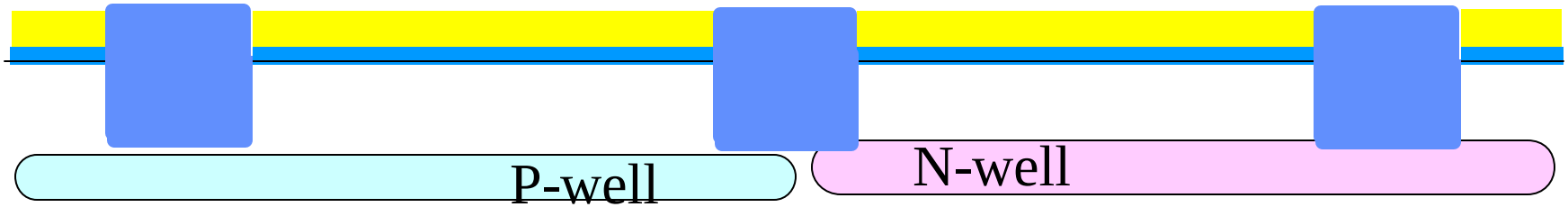
Recipe A6-FAC 0.6M TEOS
390 °C, 60 sec

CMP ENDPOINT MEASUREMENT

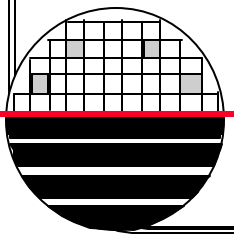


Nanospec can not measure stack of Oxide on Nitride on Oxide. So Measure (Nanospec) Oxide in Trench at start ~ 6000Å Step Height using Alpha Step of ~6000 Å Endpoint Should give Oxide in Trench of 6000Å and Step Height of zero and Nanospec of Nitride on Oxide in Active area should be ~1000Å

AFTER CMP

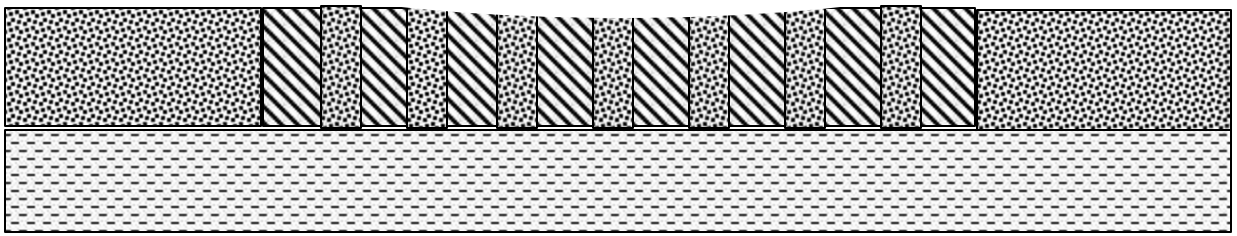


Substrate 10 ohm-cm



DISHING AND TILES

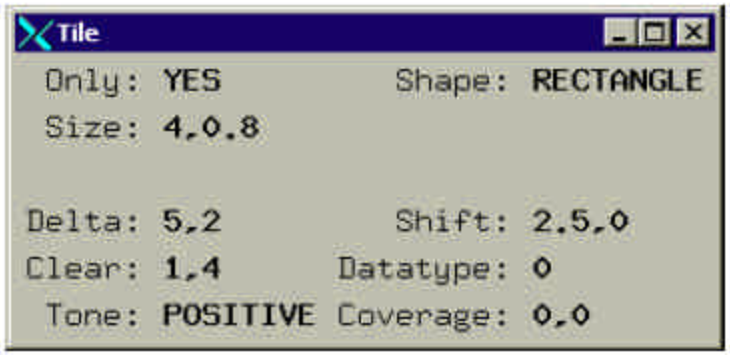
Dishing: large area becomes recessed
especially with over polishing

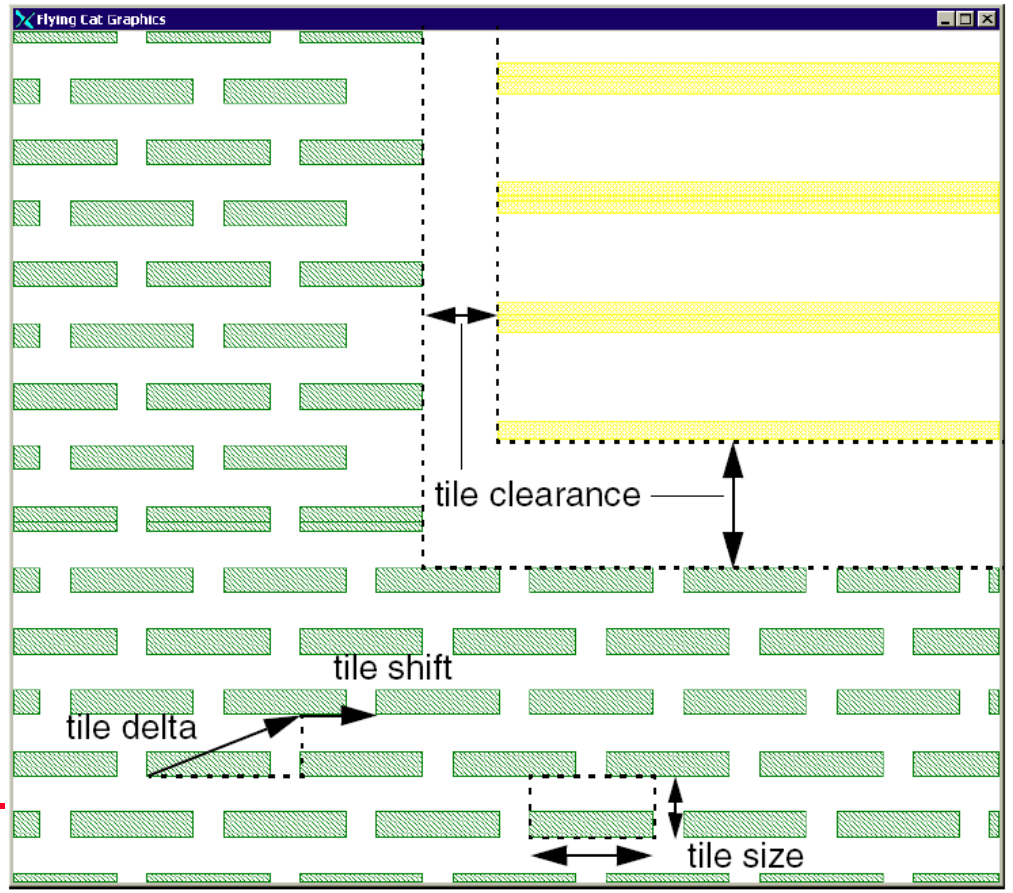


Multiple small dummy features (tiles) are used to reduce Dishing.

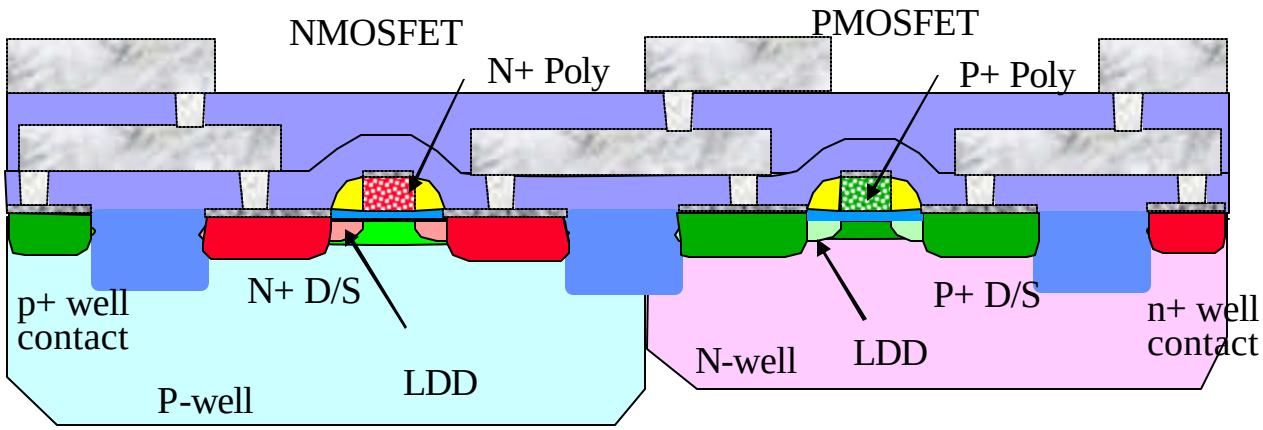
TILING FOR STI LAYER MASKMAKING

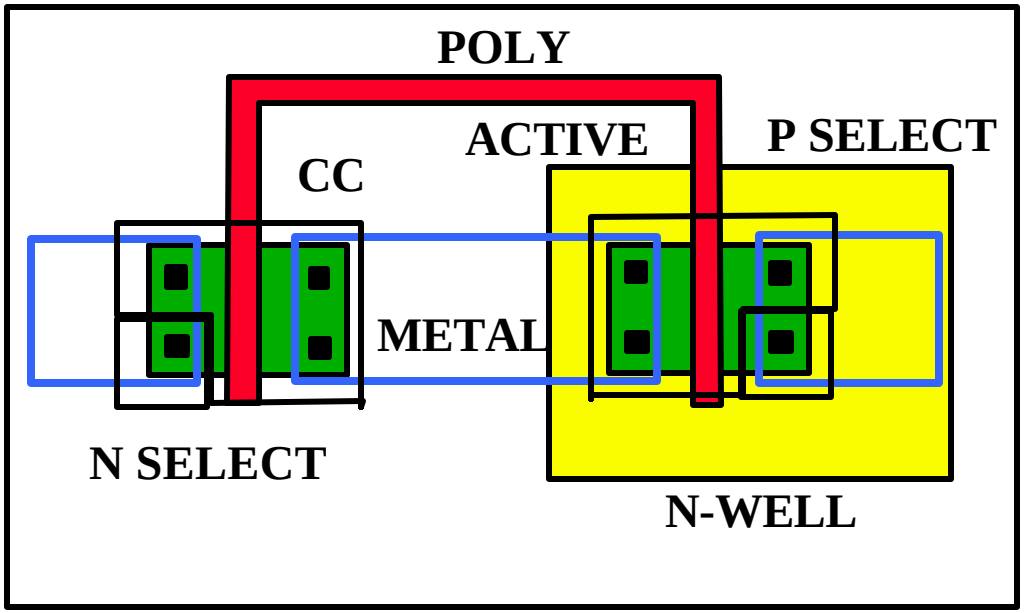
Synopsys, Inc.
CATS Software for transcription of CAD design files into readable e-beam and laser formats.

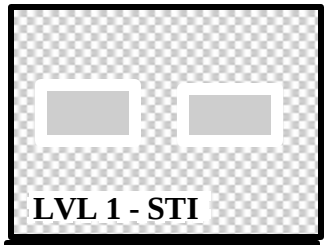


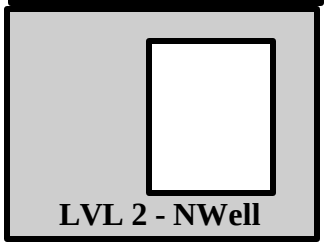


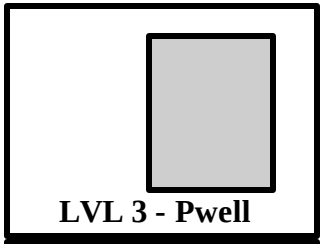
RIT ADVANCED CMOS PROCESS

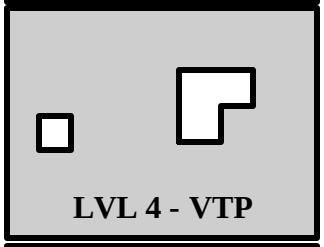


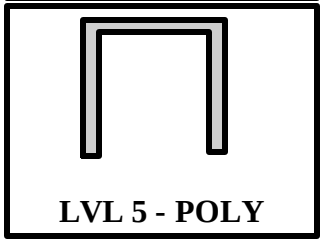




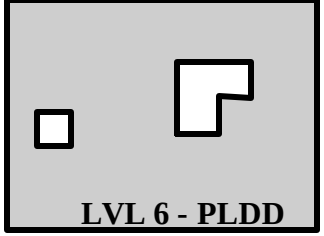


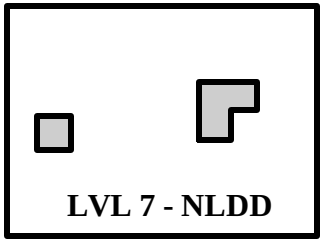


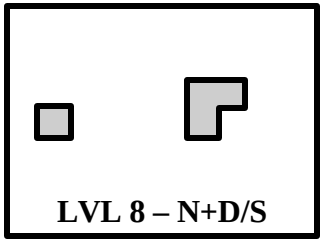


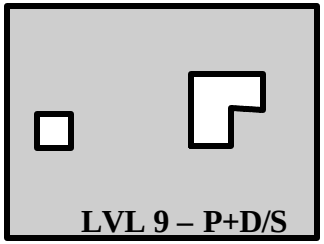


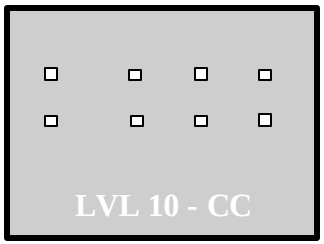
11 PHOTO LEVELS

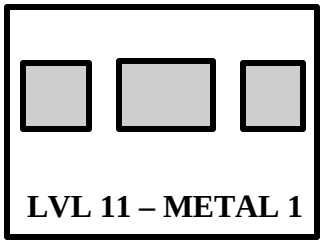




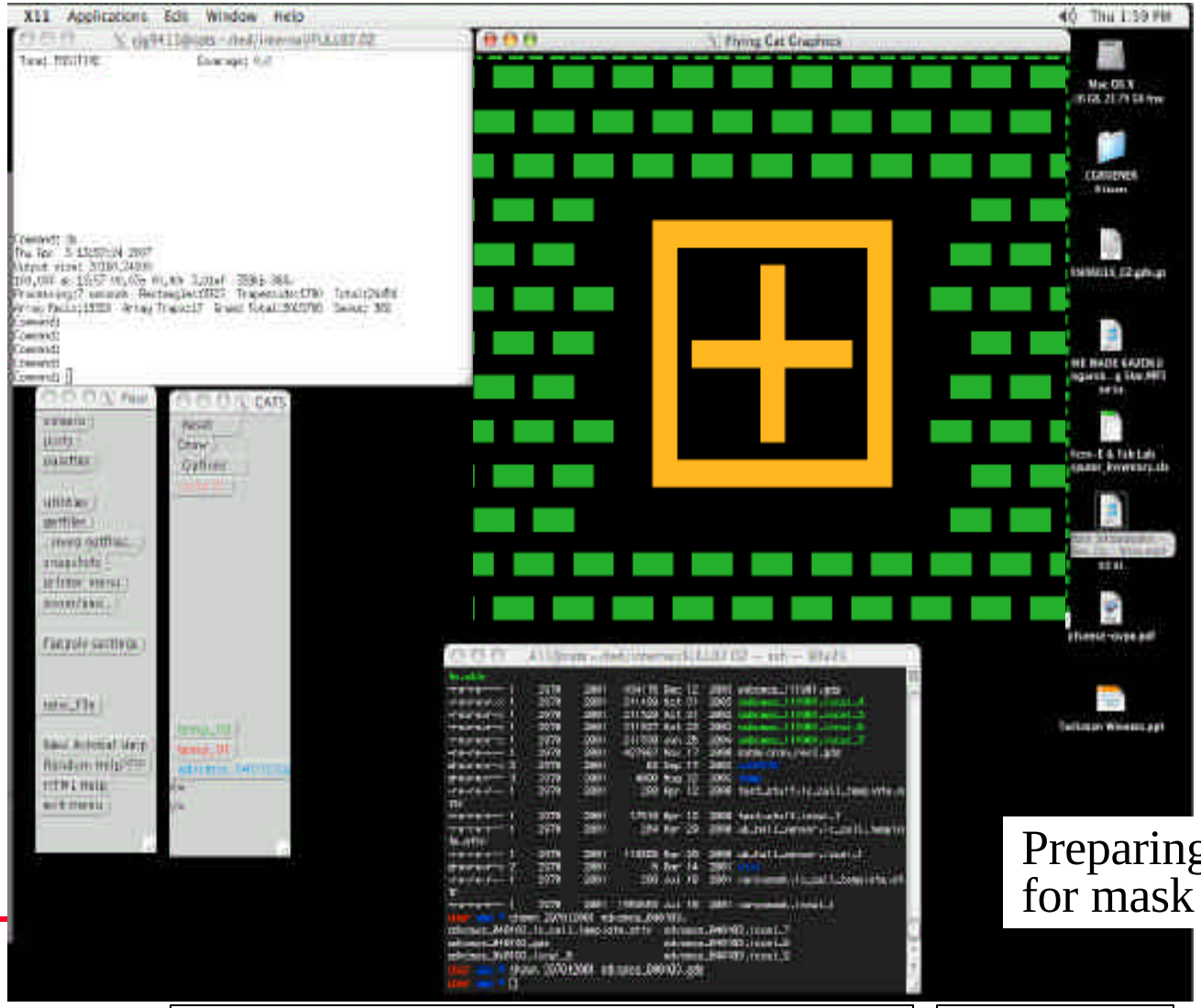








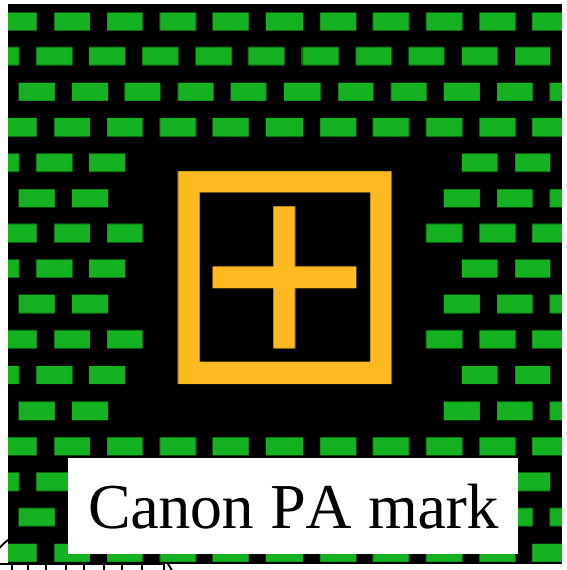
CATS



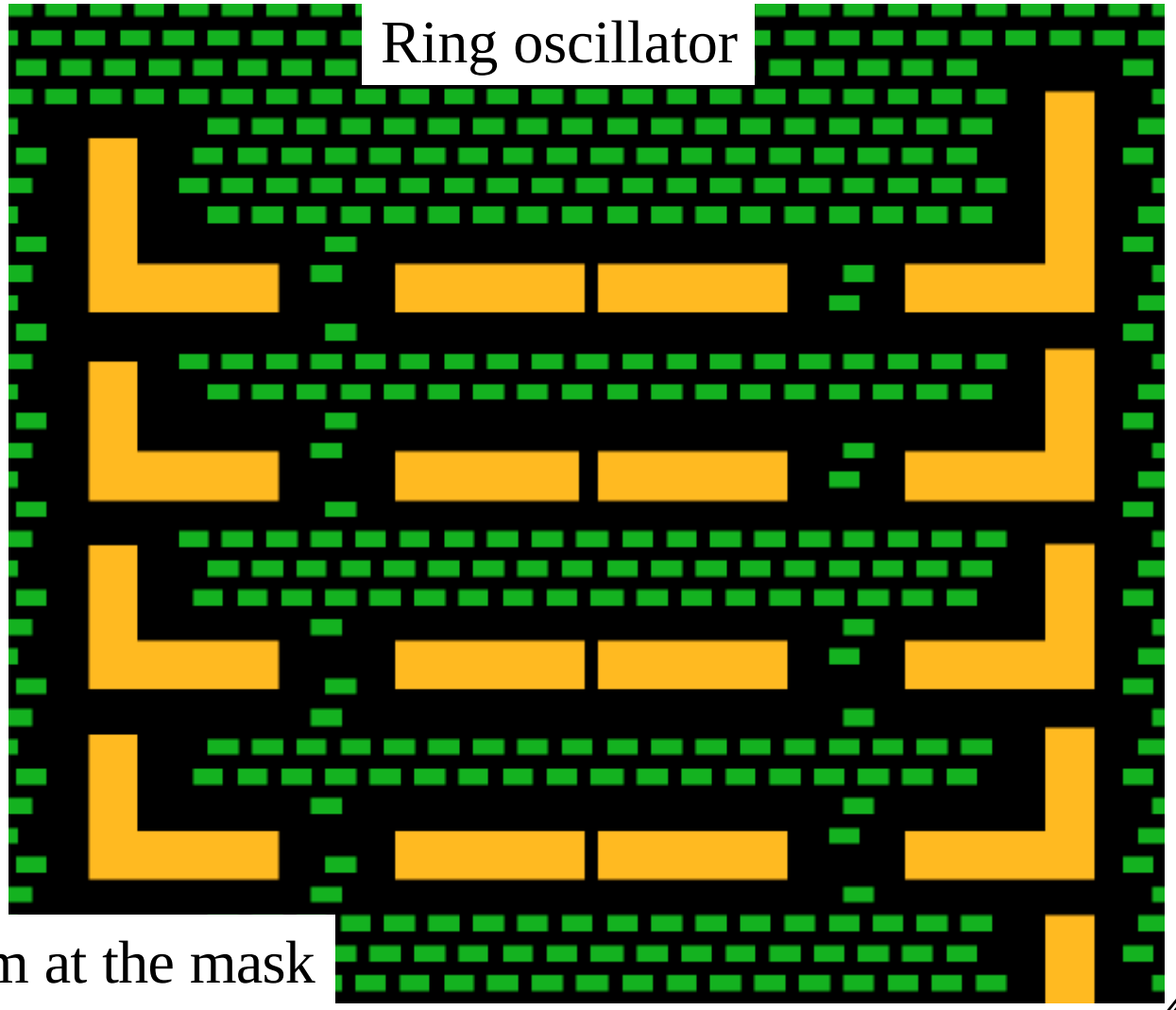
Preparing data files for mask making

TILING FOR RIT'S ADV-CMOS PROCESS STI LEVEL

COMPACT NO
TILE ONLY NO
TILE SHAPE RECTANGLE
TILE SIZE 50,25
DILE DELTA 75,50
TILE CLEAR 50,50
TILE SHIFT 25,0



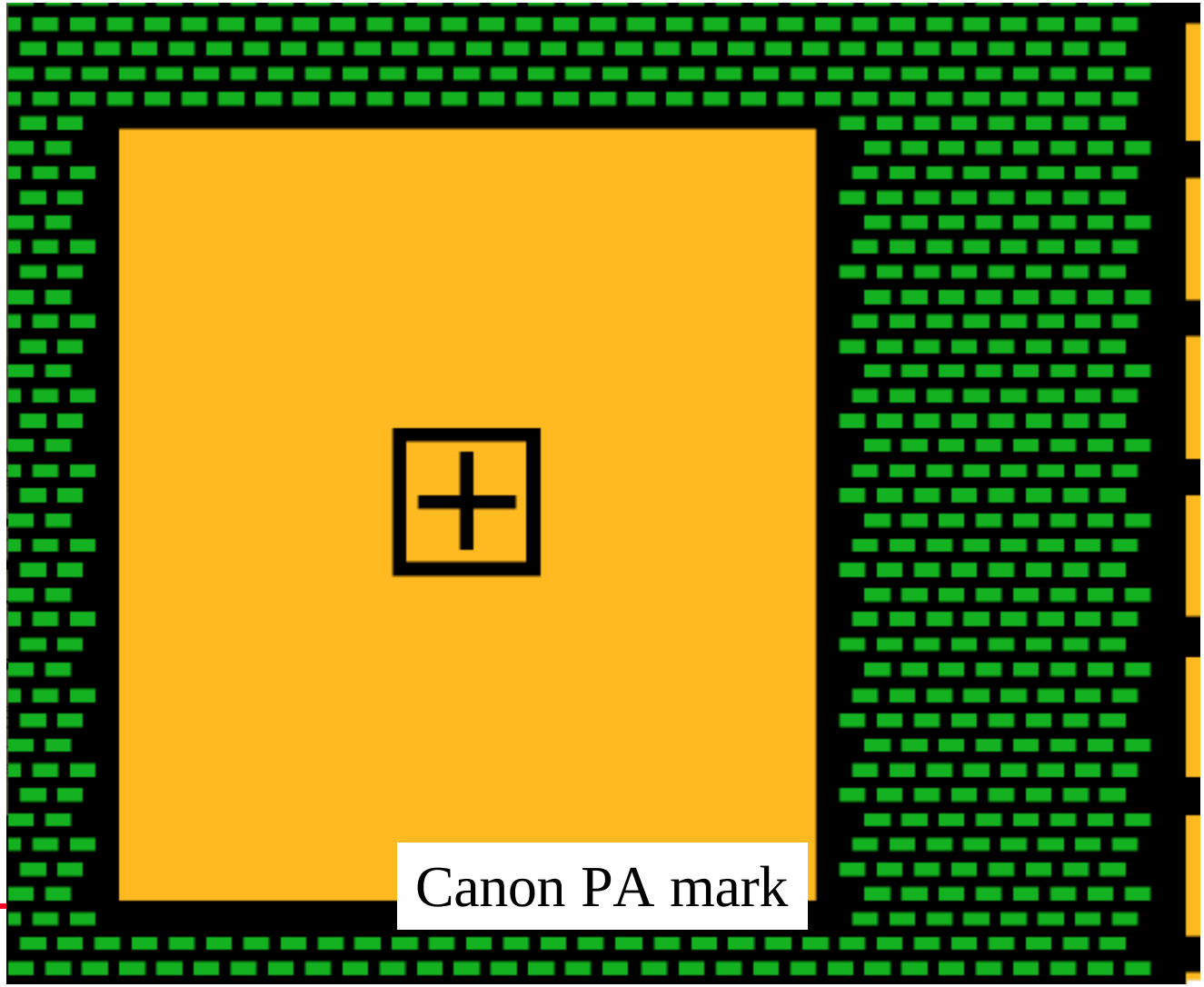
Canon PA mark



Ring oscillator

Sizes are in µm at the mask

REMOVE TILING NEAR ALIGNMENT MARKS

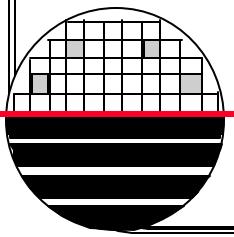


Canon PA mark

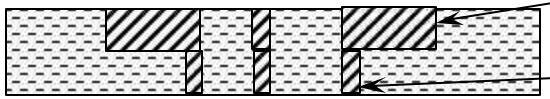
SHALLOW TRENCH ISOLATION CMP

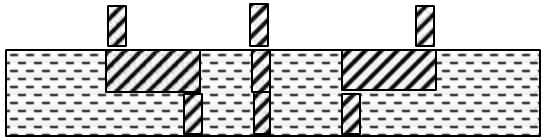
We have made great progress in doing the CMP for our advanced CMOS process shallow trench isolation (STI). The progress has been made through:

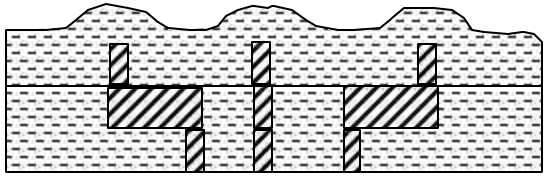
1. Getting the Westech CMP tool working correctly.
2. Getting a slurry especially made for STI that removes oxide and stops on nitride.
3. Adding tiles (dummy features) to the mask area outside of the active regions during computer aided transcription CATS prior to maskmaking. (and using tile exclusion design layer)
4. Paying attention to film stack in streets between die.

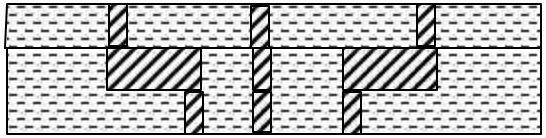


CONVENTIONAL PROCESSING TECHNOLOGY FOR MULTILEVEL METALLIZATION

1. 

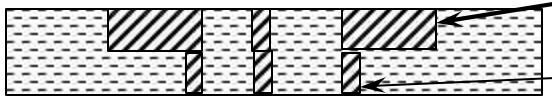
2. 
Deposit and pattern metal for via plugs

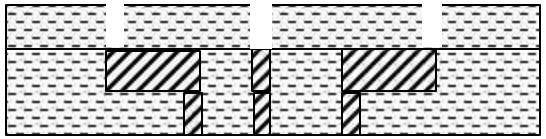
3. 
Deposit insulating film

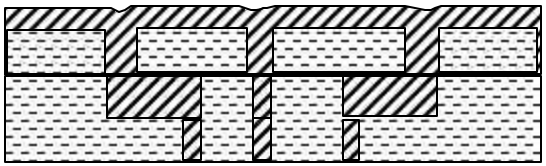
4. 
CMP insulating film

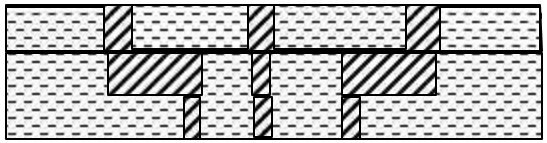
5. Repeat steps 2-5 for next level (metal lines)

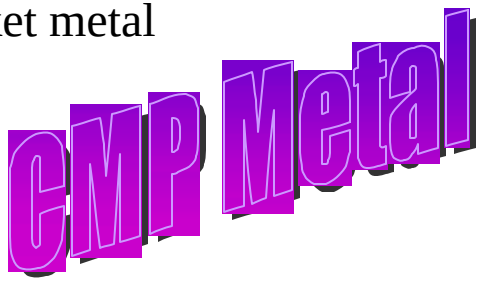
INLAID METAL (DAMASCENE) TECHNOLOGY

1. 

2. 
Deposit Dielectric and etch vias

3. 
Deposit blanket metal

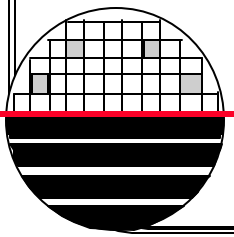
4. 
CMP metal



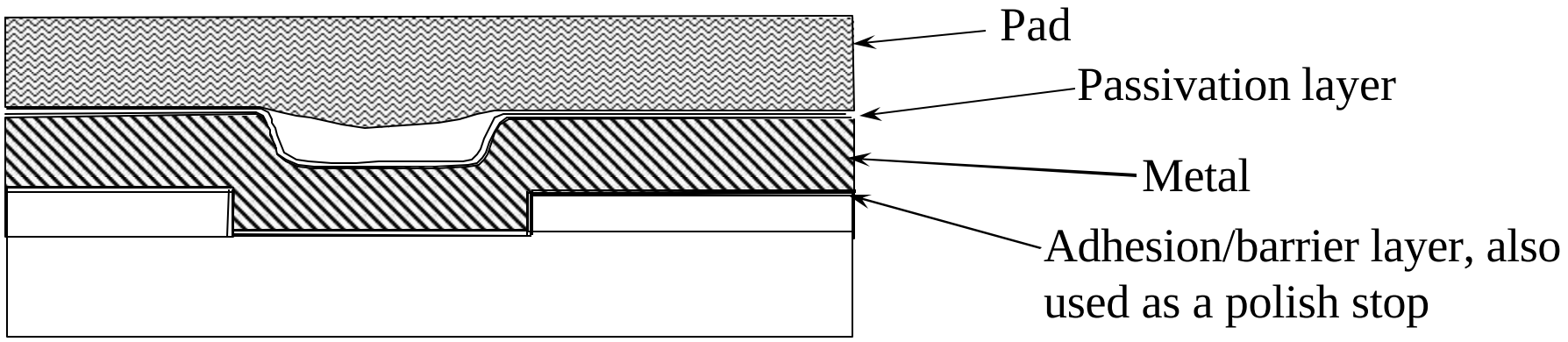
5. Repeat steps 2-5 for next level of metal lines.

METAL POLISHING

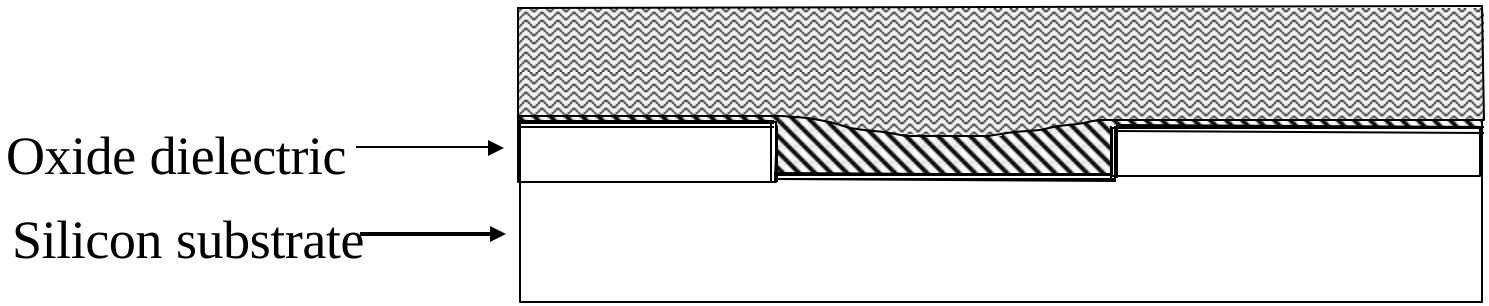
- Corrosion of the metal by the slurry (chemical)
- Passivation (self-limiting corrosion due to surface protective layer, usually oxide)
- Removal of the passivation from the high regions, from the action of the pad/slurry attrition.
- Reformation of the passivation layer on the exposed metal surfaces.



METAL POLISHING SCHEMATIC

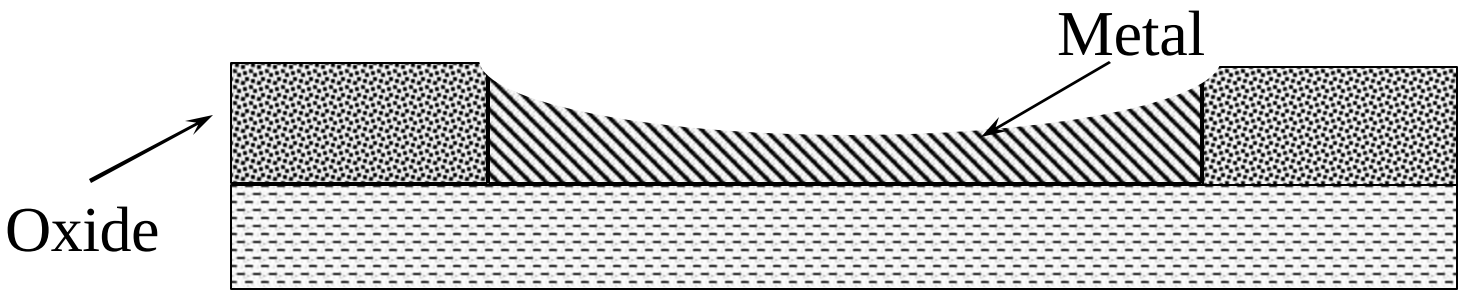


(a) Initial stage, after contact with the slurry and the resultant formation of a passivation layer, usually a metal oxide.

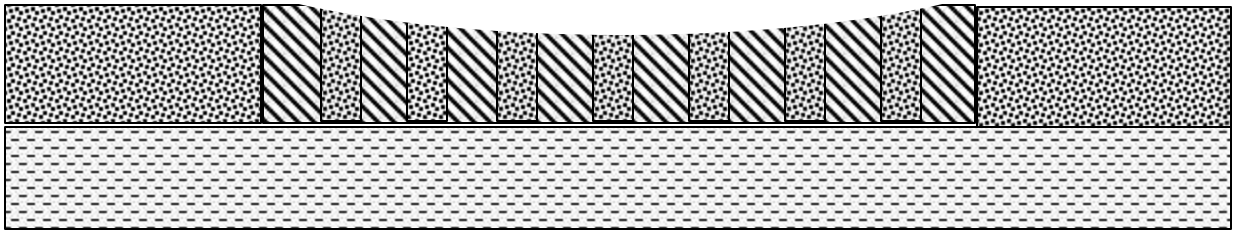


(b) Final stage of polishing. Pad is in contact with the polish stop/barrier layer.

DISHING AND EROSION

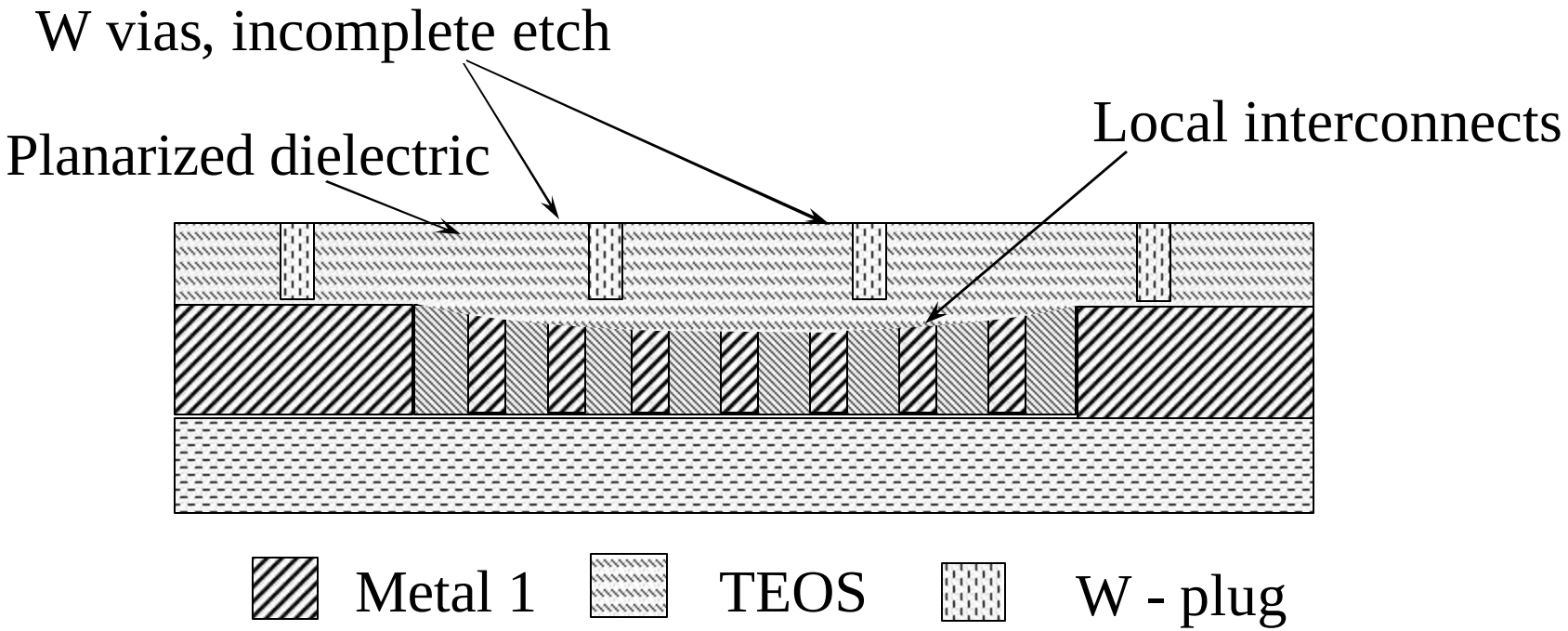


Dishing: the faster polishing material becomes recessed especially with over polishing



Erosion: Multiple small features polish faster than large features. As the amount of fast polishing material increases, erosion increases.

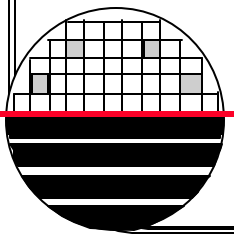
RESULT OF W-CMP EROSION



Dishing adds demands on deep via etching, plus the depth of focus problem

DESIGN IMPLICATIONS OF METAL DISHING AND EROSION

- Large metal features will dish severely
- Oxide supporting structure will reduce dishing; therefore dummy features are effective.
- The more oxide supporting features, the less erosion.
- Trade-off between metal conductivity and planarity.
- Problem areas:
  - Alignment marks, test structures, power lines, layout complexity.



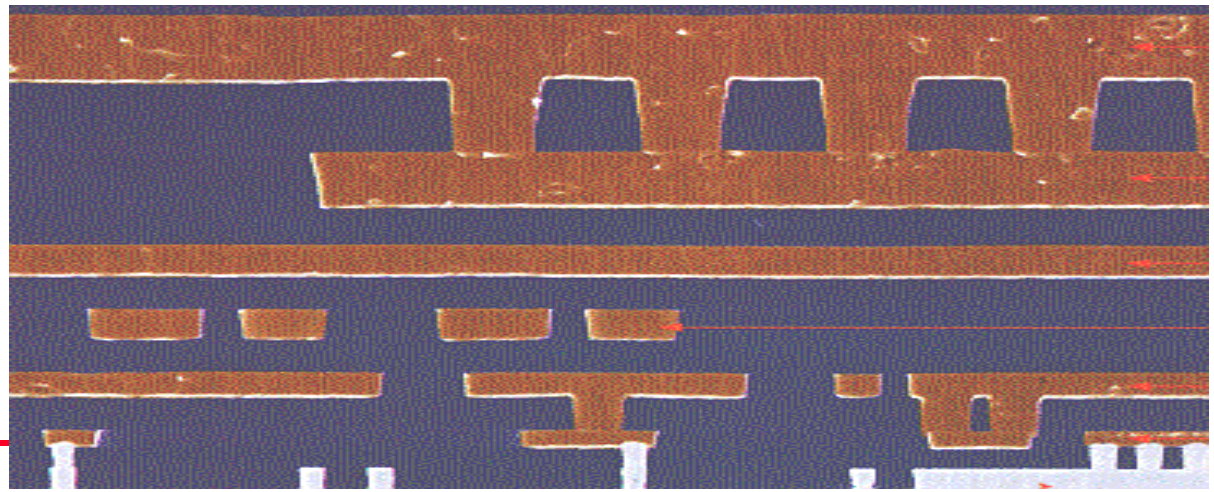
COPPER INTERCONNECTS

Advantages:

Cu has excellent conductivity 1.7 μΩ-cm (Al: 3.0 μΩ-cm)
Cu = 10x electromigration resistance compared to Al.
Lower manufacturing cost (assuming dual Damascene)

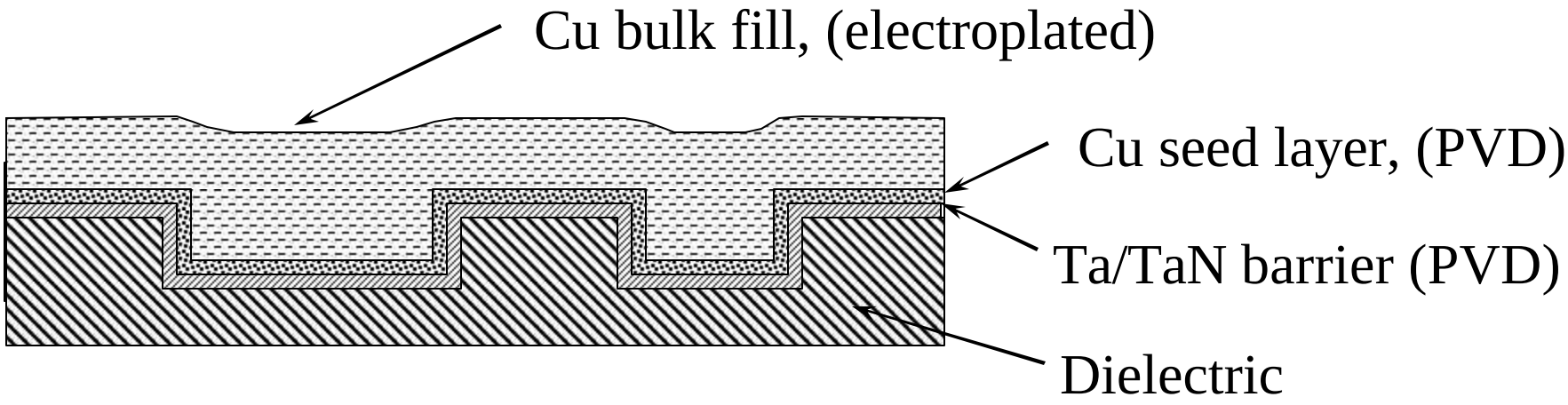
Disadvantages:

Cu diffuses fast, poisons silicon, requires good barrier layer.
No proven plasma etching process, requires damascene process.
CVD deposition is difficult, needs alternative dep. process.



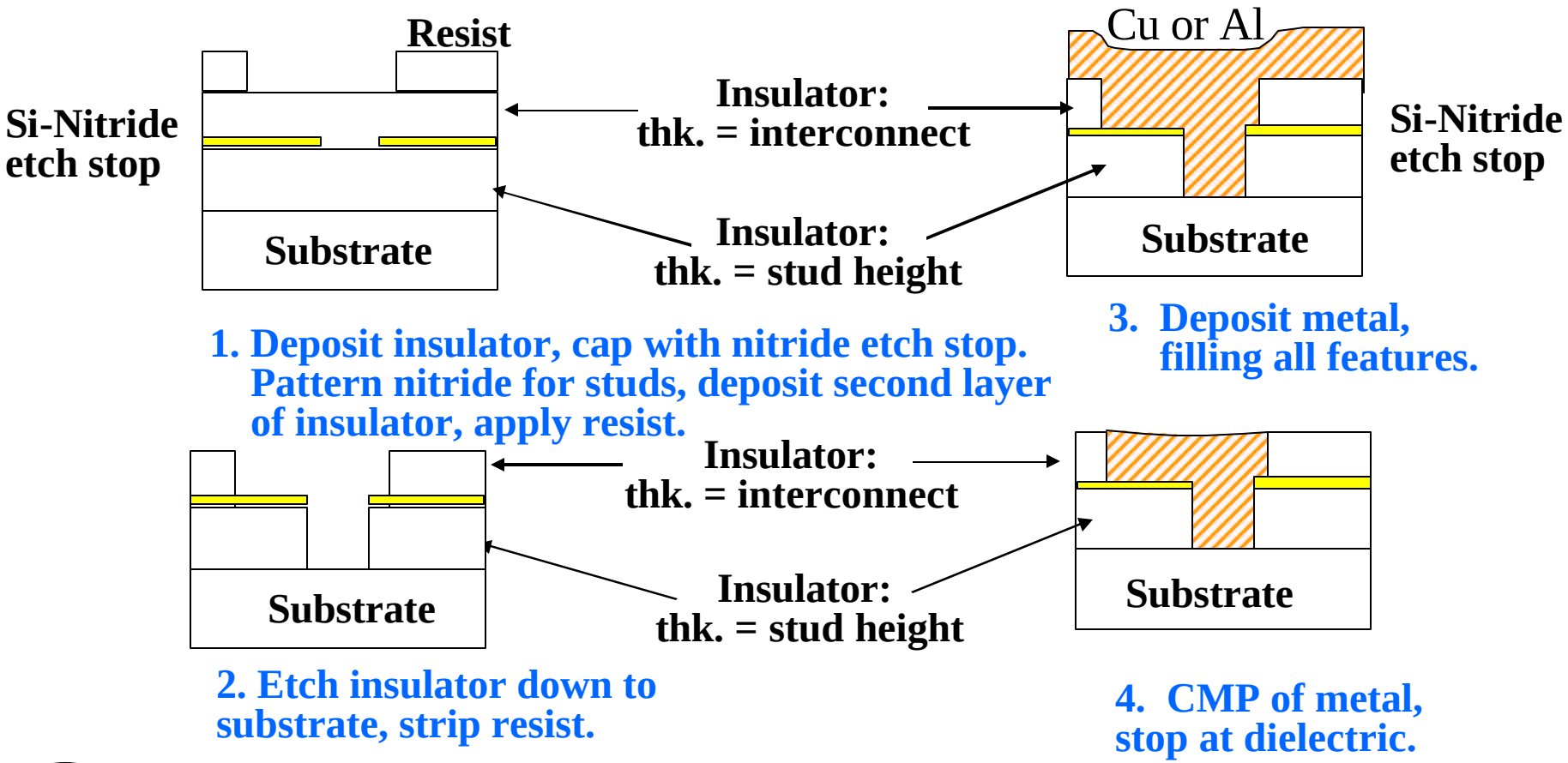
COPPER INTERCONNECT STRUCTURE

"Next year, the use of copper will be fairly widespread"
Singer, P., June (1998)



Another promising barrier layer is tungsten nitride.

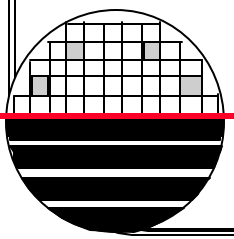
DUAL INLAID METAL (DUAL DAMASCENE)



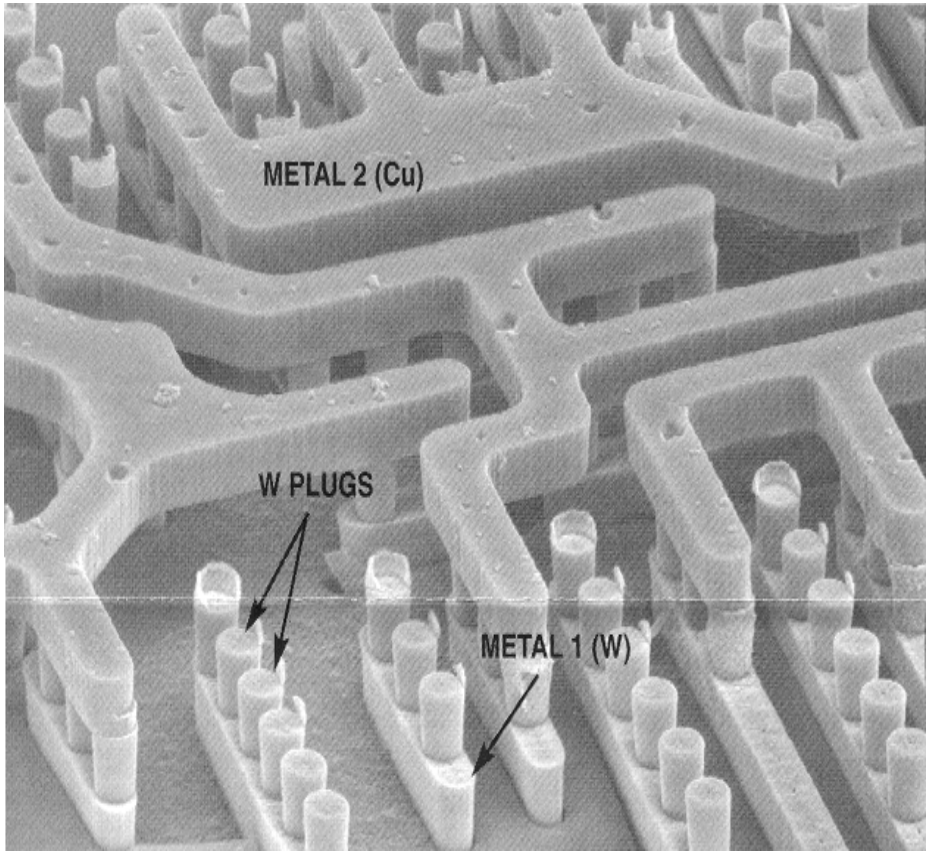
Dual approach requires 20-30% fewer steps than traditional subtractive patterning.

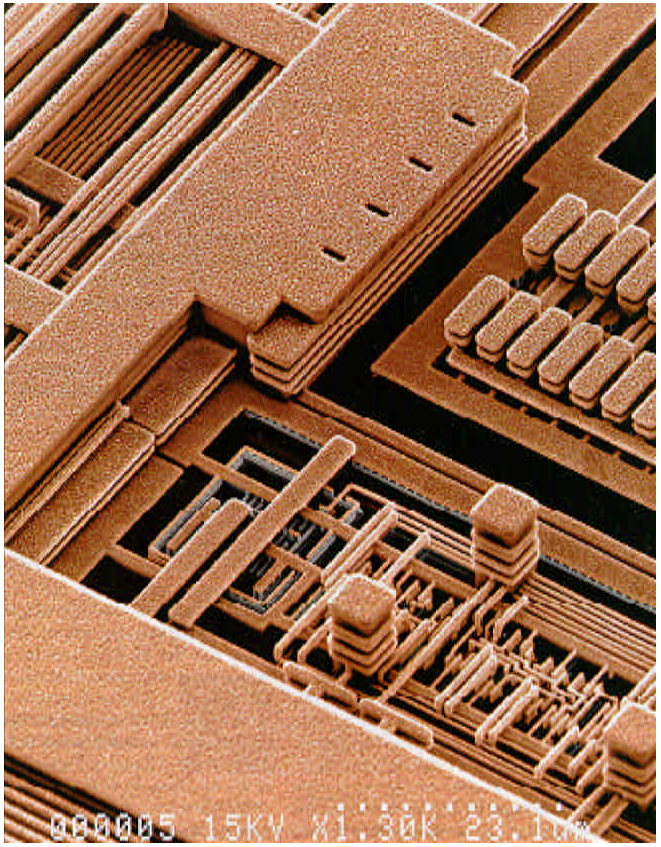
CU DEPOSITION METHODS

- **PVD: Step coverage limited, especially for sub-micron, high aspect ratio features.**
- **CVD: Conformal, uses metal-organic precurser, development required, high cost. May be required for future smaller geometries.**
- **Electroplating: Promising, good conformality and filling properties. Requires seed layer deposited by PVD Not a commonly used method in IC processing.**
- **Electroless plating: Still requires a seed layer, (conductive material)**



Cu INTERCONNECT





ENDPOINT DETERMINATION METHODS

Calculated Time from Measured Rate

Frictional Force Change – Motor Current

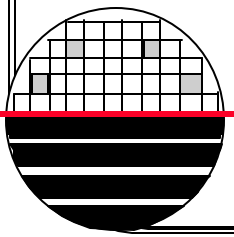
Temperature of Pad

Chemical Indicator

Electrochemical Potential

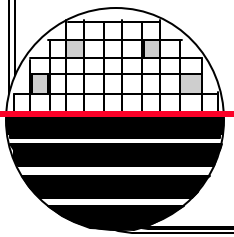
In-situ Thickness Measurement

Polish Stop Layers, Selectivity



SIGNIFICANCE OF CMP

- Current DRAMs use 3-4 layers of metal.
  - (There are two polishes at each level.)
- Average high-end ICs use four layers of metal
  - Intel up to 6 layers in 1996.
- Copper technology anticipates significantly more metal levels, but only one polish per level.
  - (Assuming dual damascene process.)
- CMP is widely accepted now, after the industry overcame the old paradigm of always keeping the wafer clean.
- CMP adds cost, ($7-10 per wafer) but its ability to enhance other processing steps while improving circuit performance results in a significant overall benefit.



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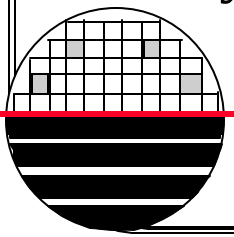

HOMEWORK - CMP

Visit your CMP area or interview a CMP expert and determine:

1. Type of equipment used.
2. How endpoint is determined.
3. What pads and slurry are used.
4. When are the pads replaced.
5. What different processes are done. (e.g. what is different when CMP oxide, CMP metal, etc.)