Chemical Vapor Deposition

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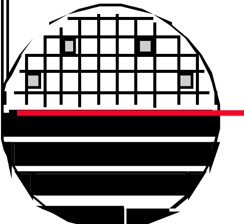

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OUTLINE

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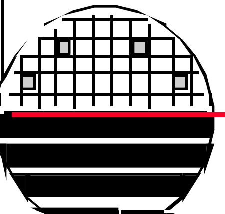

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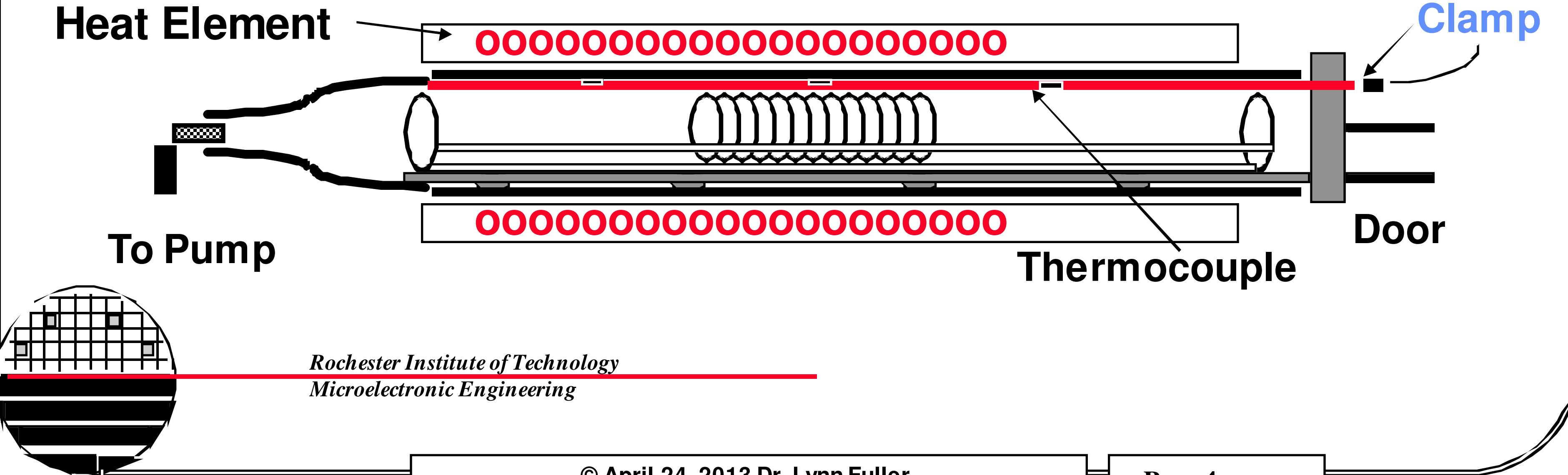
INTRODUCTION

Chemical vapor deposition is a technique for depositing thin films of materials on wafers or other substrates. Source gases are introduced into a reaction chamber and energy is applied through heat, high frequency high voltage (RF Power), or other techniques that result in the decomposition of the source gas and reaction of the chemicals to form a film.

VARIATIONS OF CVD

Epitaxy – APCVD, LPCVD or MBE (PVD)
APCVD - Atmospheric Pressure CVD
LPCVD - Low Pressure CVD
PECVD - Plasma Enhanced CVD
MOCVD - Metal Organic CVD
PVD – Physical Vapor Deposition (not a CVD process)



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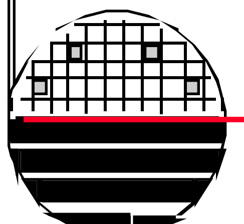
CVD CHEMISTRY

Epi	$SiCl_4 + 2H_2 \longrightarrow Si + 4HCl$
Polysilicon	SiH_4 (gas) $\longrightarrow$ Si (solid) + $2H_2$
Silicon Nitride	$SiCl_2H_2 + NH_4 \longrightarrow Si_3N_4 + HCl$
Low Temperature Oxide	$SiH_4 + O_2 \longrightarrow SiO_2 + H_2$
Tungsten (Selective on Si not on SiO2)	$WF_6 + 3H_2 \longrightarrow W + 6HF$
TEOS (tetraethyl orthosilicate)	$Si(C_2H_5O)_4 \longrightarrow SiO_2 + 4C_2H_4 + 2H_20$

TiN (TDMAT) reduction of $Ti[N(CH_2CH_3)_2]_4$



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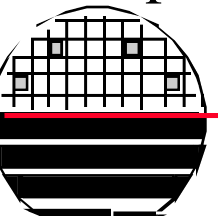
EPITAXIAL LAYER GROWTH

Epitaxial Layer Growth is the formation of single crystal material on a single crystal substrate.

$$SiCl4 + 2H2 \rightleftarrows Si + 4\ HCl$$

Allows lightly doped layers to be grown on top of heavily doped material, which is impossible through diffusion. Thickness from 1 to 20 micrometers and doping from 1E15 cm-3 to 1E17 cm-3

Deposition rate of 0.4 to 1.5 microns/minute at 1150-1230 °C



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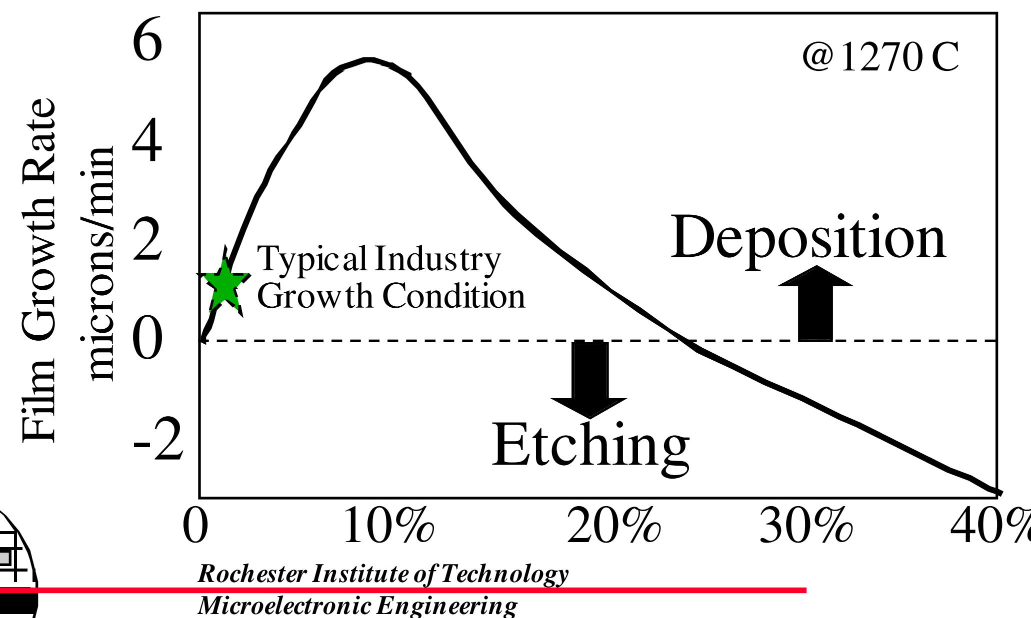
THE EFFECT OF GAS RATIO ON THE REACTION

Depostion: $SiCl_4$(gas) + $2H_2$(gas) ⇄ Si(solid) + 4 HCl(gas)

Etching: Si(solid) + $SiCl_4$(gas) ⇄ $2SiCl_2$(gas)

Growth Rate of Silicon vs. Mole Fraction of SiCl4



Mole Fraction of SiCl4

$$\frac{SiCl4}{SiCl4 + H2}$$

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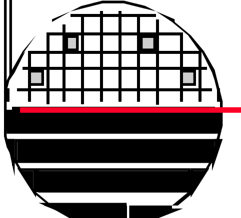
OTHER EPITAXIAL LAYER GROWTH CHEMISTRIES

$SiCl_4$ silicon tetrachloride, deposition rate of 0.4-1.5 µm/min @ 1150-1250 °C
$SiHCl_3$ trichlorosilane, deposition rate of 0.4-2.0 µm/min @ 1100-1200 °C
SiH_2Cl_2 dichlorosilane, deposition rate of 0.4-3.0 µm/min @ 1050-1150 °C
SiH_4 silane deposition rate of 0.2-0.3 µm/min @ 950-1050 °C

$SiCl_4$
- High Growth Rate
- High Temperature
- Wafer Warpage
- Out Diffusion

SiH_4
- Low Temp
- Low Growth Rate
- More Dangerous



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SELECTIVE EPITAXIAL-CHANNEL MOSFET

An 0.18-μm CMOS for Mixed Digital and Analog Applications with Zero-Volt-V_{th} Epitaxial-Channel MOSFET's

Tatsuya Ohguro, *Member, IEEE*, Hiroshi Naruse, Hiroyuki Sugaya, Eiji Morifuji, *Member, IEEE*, Sinichi Nakamura, Takashi Yoshitomi, *Member, IEEE*, Toyota Morimoto, Hideki Kimijima, Hisayo Sasaki Momose, *Member, IEEE*, Yasuhiro Katsumata, *Member, IEEE*, and Hiroshi Iwai, *Fellow, IEEE*

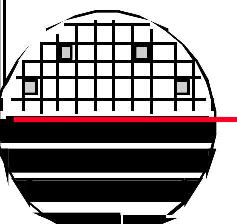
***Abstract*—An 0.18-μm CMOS technology with multi-V_{th}'s for mixed high-speed digital and RF-analog applications has been developed. The V_{th}'s of MOSFET's for digital circuits are 0.4 V for NMOS and −0.4 V for PMOS, respectively. In addition, there are n-MOSFET's with zero-volt-V_{th} for RF analog circuits. The zero-volt-V_{th} MOSFET's were made by using undoped epitaxial layer for the channel regions. Though the epitaxial film was grown by reduced pressure chemical vapor deposition (RP-CVD) at 750 °C, the film quality is as good as the bulk silicon because high pre-heating temperature (940 °C for 30 s) is used in H_2 atmosphere before the epitaxial growth. The epitaxial channel MOSFET shows higher peak g_m and f_T values than those of bulk cases. Furthermore, the g_m and f_T values of the epitaxial channel MOSFET show significantly improved performances under the lower supply voltage compared with those of bulk. This is very important for RF analog application for low supply voltage. The undoped-epitaxial-channel MOSFET's with zero-V_{th} will become a key to realize high-performance and low-power CMOS devices for mixed digital and RF-analog applications.**

The sacrifice oxide was removed selectively in the analog n-MOSFET area by using a mask step [Fig. 1(b), (ii)]. Then, undoped epitaxial Si layer of 30 nm was grown selectively on this area by RP-CVD [Fig. 1(b), (iii)]. The process conditions of RP-CVD are listed in Table III. Just prior to the deposition, the native oxide layer was evaporated by using *in situ* high-temperature pre-heating at 940 °C for 30 s in H_2 atmosphere. A 30 nm intrinsic or undoped silicon epitaxial layer was grown at 750 °C by using SiH_2Cl_2 gas. The growth rate is 2 nm/min.

SOS - SILICON ON SAPPHIRE

Thin layer of epitaxial single crystal silicon, combined with trench isolation, to make isolated devices

Starting Saphire wafer, Al_2O_3, Single crystal and a Silicon epitaxial layer can be grown on it.



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SIMOX -SEPARATION BY ION IMPLANTED OXYGEN

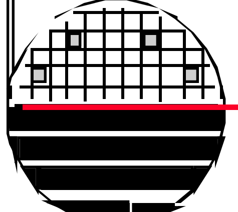
Implanted Oxygen or Nitrogen Ions

Thin layer of single crystal silicon, combined with trench isolation, to make isolated devices

1 Million Electron Volt, High Dose (2E18) Implant, to Make a Buried Dielectric Layer of SiO_2 or Si_3 N_4 , Also 200KeV, High Dose Implant followed by anneal and Epitaxy Growth

CRYSTALLINITY

- Amorphous - No recognizable long-range order
- Polycrystalline - Completely ordered in small domains, disjoint or misoriented from one another
- Crystalline - The entire solid is made up of atoms in an orderly array. The overwhelming number of devices made today use crystalline silicon.
- Thin film transistors for applications like liquid crystal displays can be made in amorphous or polycrystalline material, but suffer from degraded material and electrical properties.
- In general, it takes more energy (usually as heat) to create a more ordered material. For example, silane decomposition in an LPCVD furnace at 550°C results in amorphous silicon whereas the same process at 610°C results in polysilicon deposition.
- Much higher temperatures are needed to grow silicon epitaxially (follows the substrate crystal structure). You can only grow single crystal silicon on a silicon crystal (or something very close such as sapphire).



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POLY SILICON DEPOSITION BY LPCVD

Polysilicon is used as a gate material, for resistors and for capacitors. In EEPROM's and CCD's two layers of overlapping poly is used in the basic structure. Poly can withstand high temperatures and as a result can be deposited prior to drain and source formation. Poly can be deposited undoped and doped later by diffusion or ion implantation or it can be deposited and doped at the same time (insitu)

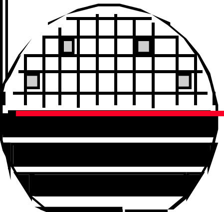
$$SiH_4 = Si + 2H_2$$

RIT 6" LPCVD Tool, Poly 610°C Polysilicon Deposition (undoped):

Temperature = 610 °C
Pressure = 300 mTorr
Gas = Silane (SiH4)
Flow = 100 sccm
Rate = 75 Å/min

RIT 6" LPCVD Tool, Poly 650°C Polysilicon Deposition (undoped):

Temperature = 650 °C
Pressure = 300 mTorr
Gas = Silane (SiH4)
Flow = 100 sccm
Rate = 120 Å/min

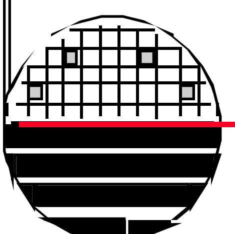


SILICON NITRIDE BY LPCVD

Films can be deposited up to about 5000 Å directly on silicon before the stress is so large that the film fractures (Dr. Lane, Dr. Fuller). Pad oxide under the nitride film and special silicon rich nitride films may allow nitride film thickness over 5000 Å.

$$3SiH_2Cl_2 + 4NH_3 = Si_3N_4 + 9H_2 + 3Cl_2$$

RIT 6" LPCVD Tool
Silicon Nitride (Si3N4) (stociometric):
Temperature = 810 °C
Pressure = 400 mTorr
Dichlorosilane (SiH2Cl2), Flow = 60 sccm
Ammonia (NH3), Flow = 150 sccm
Rate = 60 Å/min +/- 10 Å/min
Recipe: Factory Nitride 810



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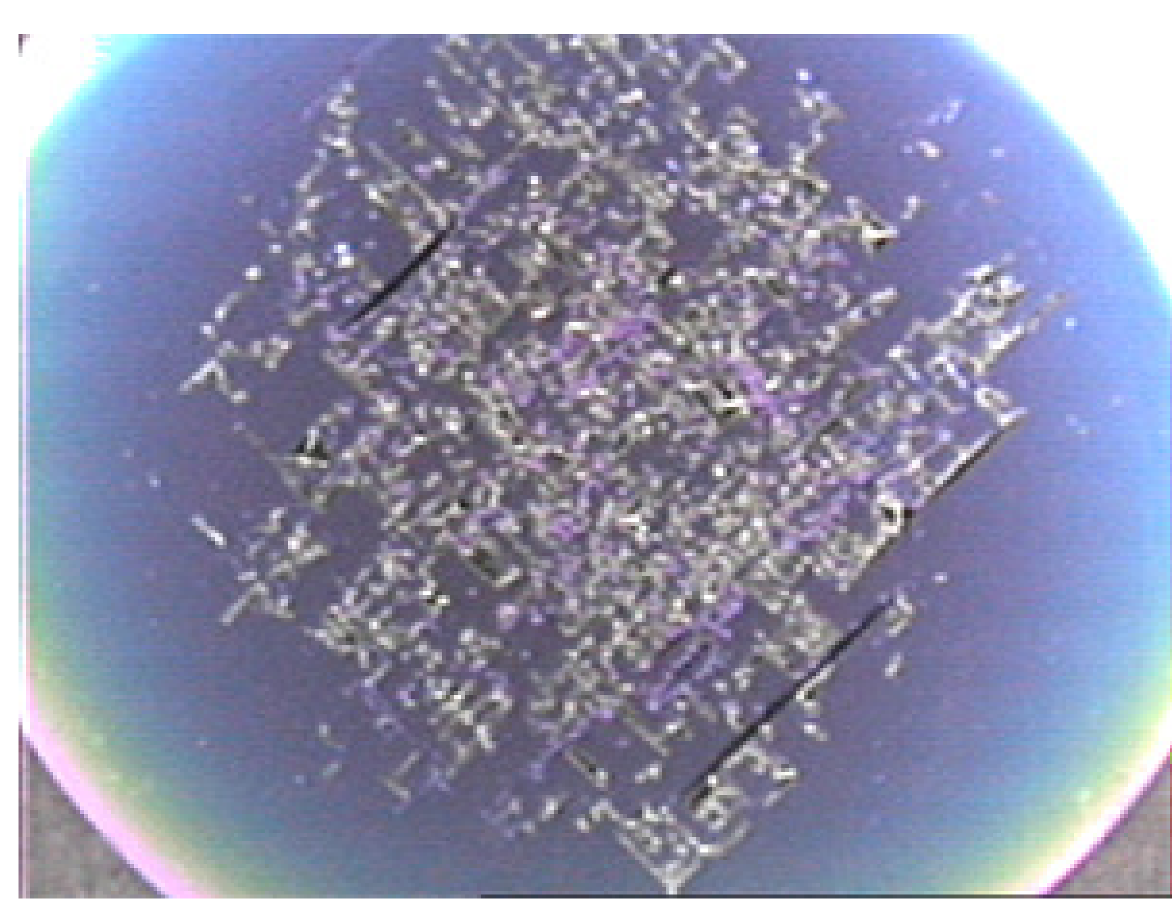
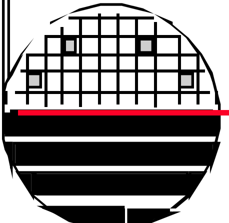
STRESS IN SILICON NITRIDE FILMS

Stress in an 8000 A Nitride Film





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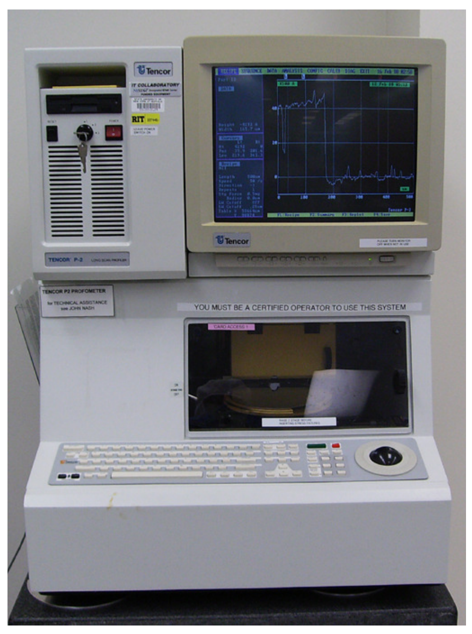
FILM STRESS IN SILICON NITRIDE

Kenneth L. Way, Jr. did his senior project on stress in silicon nitride films as a function of the ratio of ammonia to dichlorosilane. Samples were coated with flows as follows and stress was measured at ADE corporation. The silicon nitride was etched off of the backside of the wafer so that the stress curvature was due to the layer on the front side only.

Tencore P2



Flow	Stress x E 9 dynes/cm2
10:1	14.63
5:1	14.81
2.5:1	12.47
1:1	10.13
1:2.5	7.79
1:5	3
1:10	0

Stress; R = (E/(6(1-v)))*(d^2/(Rt))
where E is Youngs modulus, v is Poissons ratio, d and t are substrate and film thickness
R is negative for tensile

Compressive Stress

Tensile Stress

Also see: T.H Wu, “Stress in PSG and Nitride Films as Related to Film Properties and Annealing”, Solid State Technology, p 65-71, May 1992.

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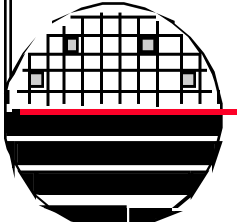
LOW STRESS SILICON NITRIDE DEPOSITION

The process details for low stress silicon nitride are NH3 flow of 4% to give 20 sccm and Dicholorosilane flow of 97% to give 200 sccm and a Deposition Pressure of 650 mTorr.

9-6-96 Dr. Fuller did a 100 min deposition giving 8100Å (center) to 8800Å (edge) nitride thickness which did not fracture due to stress. It is a definite improvement.



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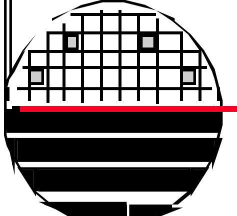
LOW TEMPERATURE OXIDE (LTO) BY LPCVD

Oxide is used as an interlevel dielectric in multilayer metal processes. Because aluminum and silicon interact at ~570 C it is necessary to deposit the interlevel dielectric at lower temperatures.

$$SiH_4 + O_2 = SiO_2 + 2H_2$$

RIT 6" LPCVD Tool
Low Temperature Silicon Oxide:

Temperature = 425 °C
Pressure = 300 mTorr
Silane (SiH4), Flow = 100 sccm
Oxygen (O2), Flow 120 sccm
Rate = 90 Å/min +/- 10 Å/min



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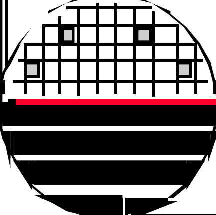
LTO USING CAGED BOAT AND INJECTOR TUBES



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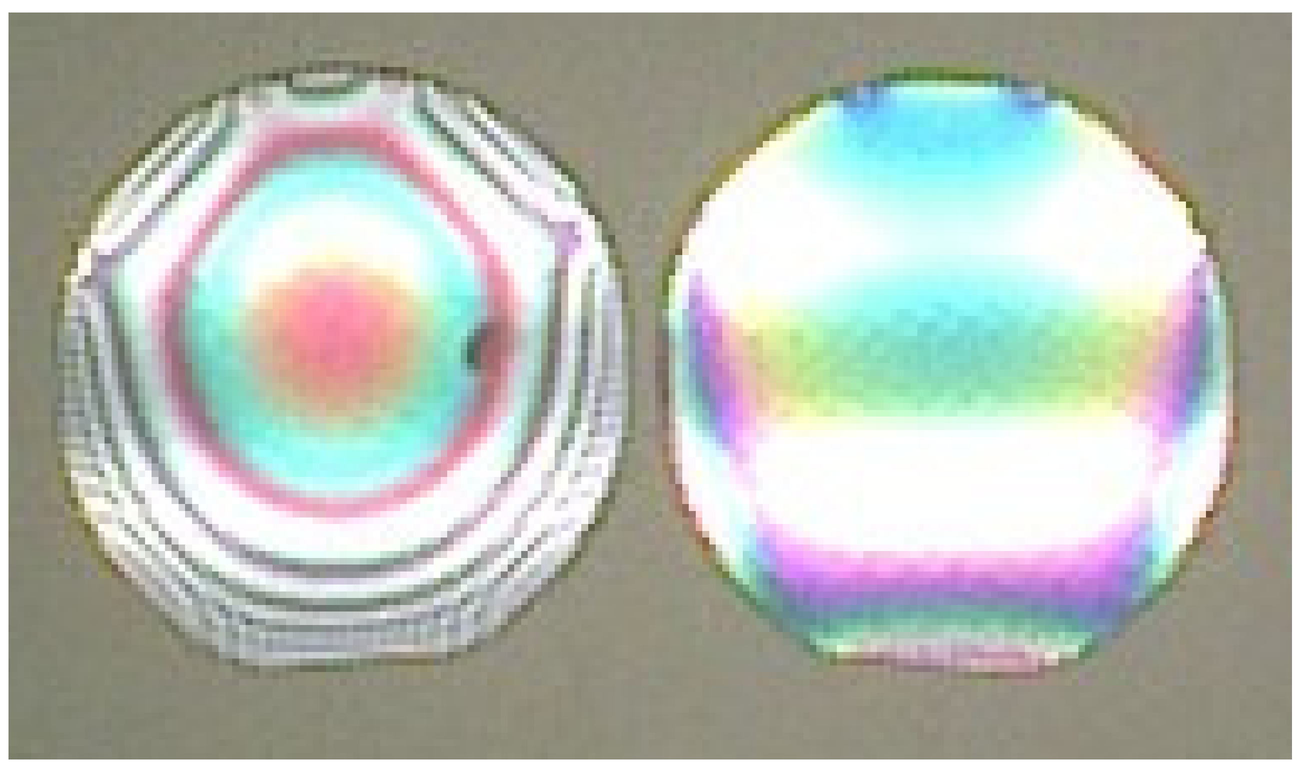
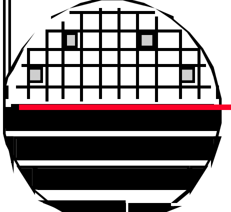
LTO



In 4” LPCVD

Using 6” LPCVD
Caged Boat and Injectors



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HTO - HIGH TEMPERATURE OXIDE

High temperature oxide is a Chemical Vapor Deposition (CVD) process that can give oxides with properties very similar to thermally grown oxide. Compared to Low Temperature Oxide (LTO) the HTO films are more uniform in thickness across the wafer, more conformal, denser, have higher dielectric strength and would be better for Shallow Trench Isolation (STI), side-wall spacers and inter-poly dielectrics than LTO.

Low Temperature Oxide (LTO)

$SiH_4 + O_2 = SiO_2 + 2H_2$

Deposition Temperature 300 to 500˚C

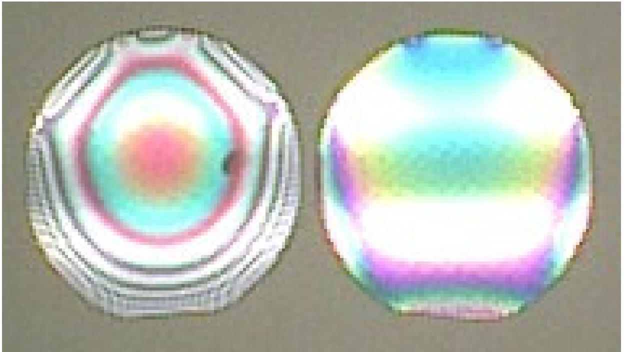
High Temperature Oxide (HTO)

$SiCl_2H_2 + 2N_2O = SiO_2 + 2N_2 + 2HCl$

Deposition Temperature 850 to 950 ˚C

No Caged Boat and Injectors

With Caged Boat and Injectors



LTO films showing poor thickness uniformity

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HTO - HIGH TEMPERATURE OXIDE

MEMS Exchange advertizes their HTO

930˚C, 360mT, Dep. Rate 50A/min

UC Berkeley advertizes

800 ˚C, DCS-20 sccm, N_2O-100 sccm, Dep. Rate 4.6A/min

RIT Process

900 ˚C, 400 mT, DCS-60 sccm, N_2O-150 sccm, Dep. Rate ~16.7A/min

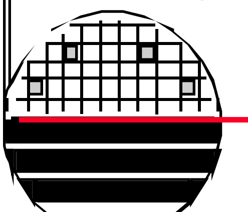
$$R = Ro * \exp\left(\frac{-E_A}{k * T}\right)$$

Activation Energy = 0.84eV

Ro = 4.9E4 Å/min and k=8.60e-5 eV/°K

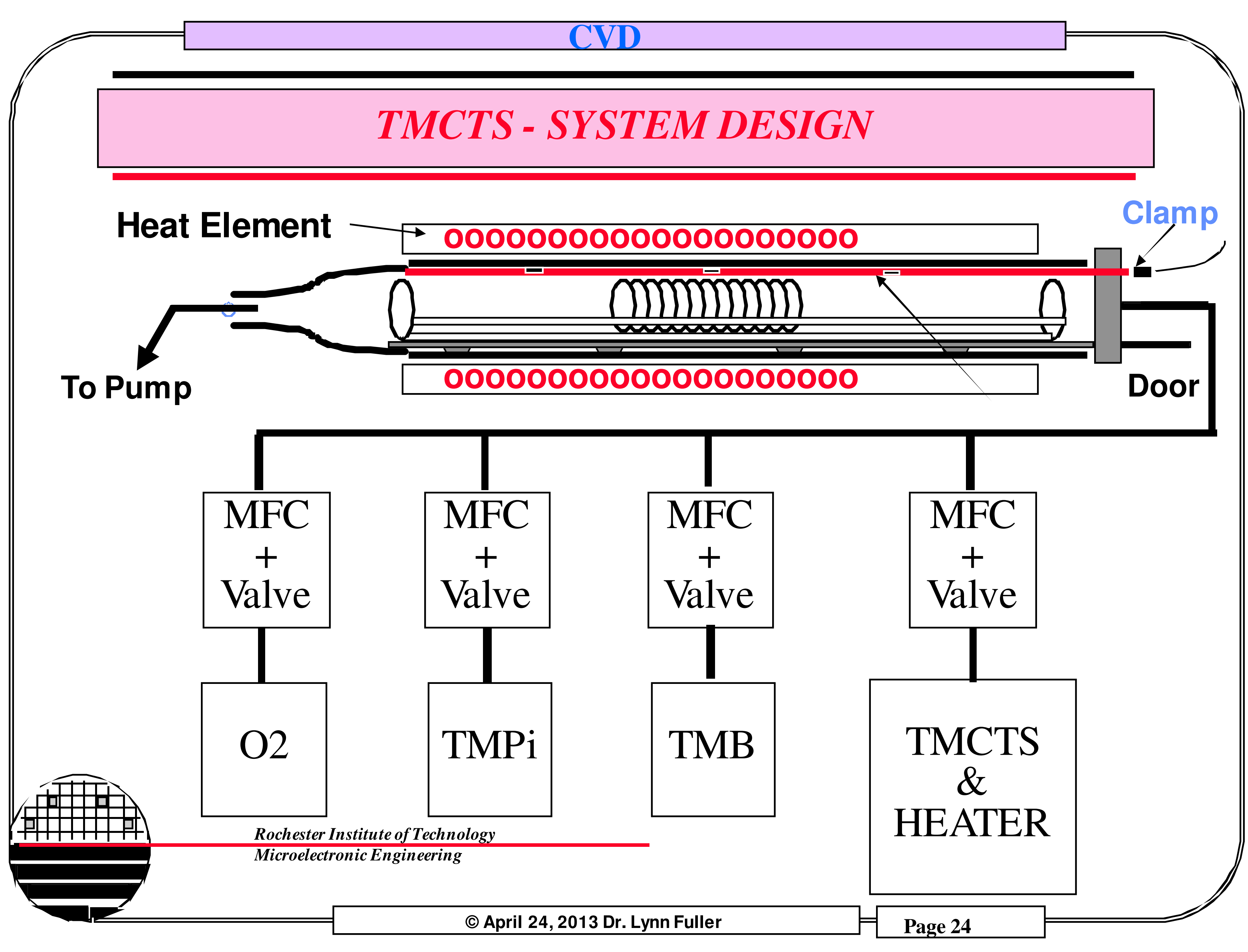
70 min Dep Results
Pattern 25
Program 02

Pt	Xox(Å)	n
1	1152	1.456
2	1192	1.454
3	1157	1.457
4	1161	1.457
5	1170	1.456



LPCVD OXIDE FROM TMCTS

TMCTS or "TOMCATS" (Tetramethylcyclotetrasilane) is a Schumacher liquid source material for low temperature deposition of undoped and doped glass. TMCTS is not pyrophoric and is non-corrosive eliminating the exposure hazards and elaborate safety equipment required for silane based processes. TMCTS reacts with O2 and other oxygen sources between 500 and 700 °C. Normally at 580 °C TMCTS provides a deposition rate ~85Å/min. TMCTS can be combined with TMPi (Trimethylphosphite) or TMB (Trimethylborate) to provide an all liquid source for deposition of BPSC (BoroPhosphoSilicate Glass)


CVD
TMCTS - SYSTEM DESIGN
Heat Element
Clamp
To Pump
Door
MFC + Valve
MFC + Valve
MFC + Valve
MFC + Valve
O2
TMPi
TMB
TMCTS & HEATER
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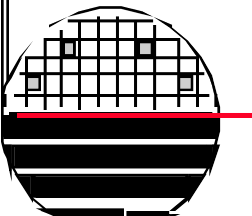
FELD - CVD SYSTEM

FELD Flash Evaporation Liquid Delivery for delivery of vaporized precursors for thin films such as:

Strontium Bismuth Tantalate $SrBi_2Ta_2O_9$
Lanthanum-modified lead zircronate titanate (PZT)
Strontium Titanate $SrTiO_3$
Barium Strontium Titanate $(Ba_{0.4}Sr_{0.6})TiO_3$

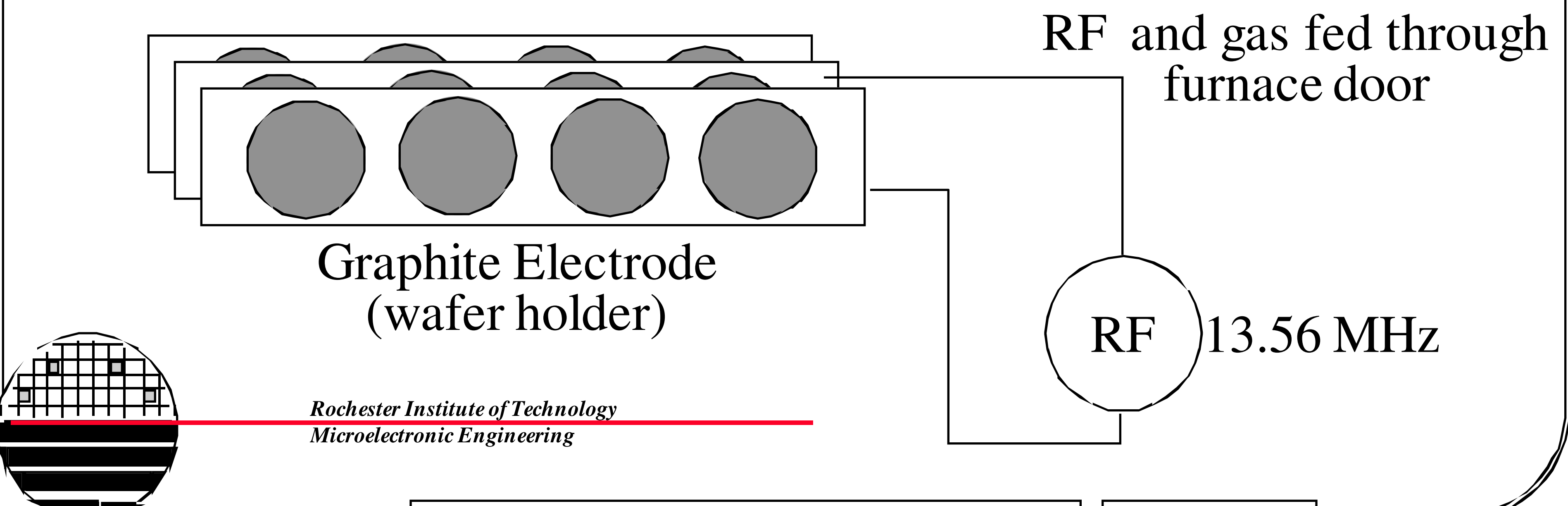
COVA
Tehnologies Inc.
www.covatech.com
(800)667-5220



PLASMA ENHANCED CVD

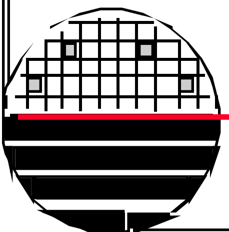
Why? LPCVD Silicon Nitride, SiH4 + NH3 @ 700-900 C
PECVD Silicon Nitride, SiH4 + NH3 @ 200-350 C

Using an RF source to create a plasma significantly reduces the deposition temperature and reduces the thermal budget



PECVD OXIDE FROM TEOS

TEOS Program: (Chamber A)
Step 1
Setup Time = 15 sec
Pressure = 9 Torr
Susceptor Temperature= 390 C
Susceptor Spacing= 220 mils
RF Power = 0 watts
TEOS Flow = 400 scc
O2 Flow = 285 scc
Step 2 – Deposition
Dep Time = 55 sec (5000 Å)
Pressure = 9 Torr
Susceptor Temperature= 390 C
Susceptor Spacing= 220 mils
RF Power = 205 watts
TEOS Flow = 400 scc
O2 Flow = 285 scc
Step 3 – Clean
Time = 10 sec
Pressure = Fully Open
Susceptor Temperature= 390 C
Susceptor Spacing= 999 mils
RF Power = 50 watts
TEOS Flow = 0 scc
O2 Flow = 285 scc



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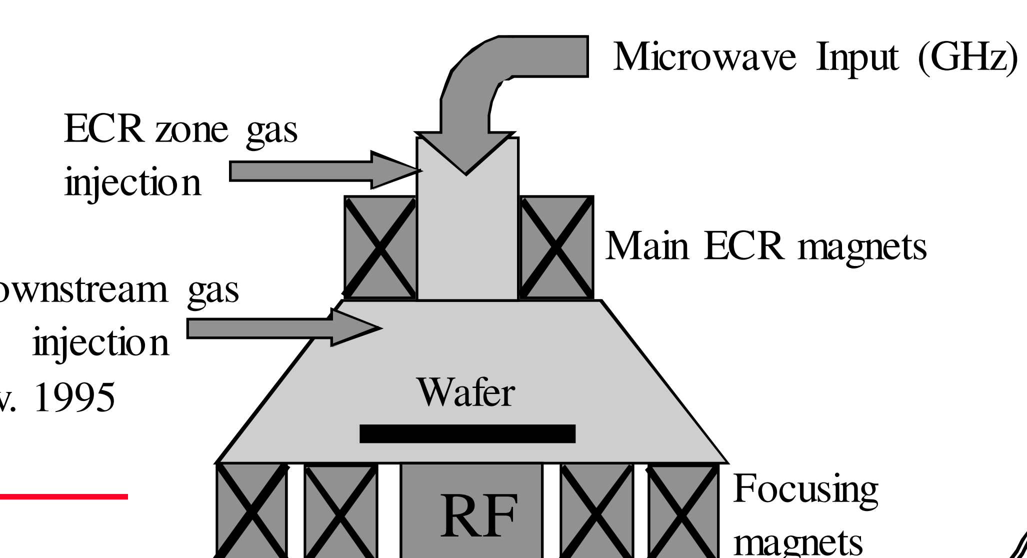
ELECTRON-CYCLOTRON RESONANCE (ECR)

Single wafer system

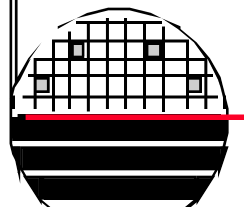
Microwave plasma within a magnetic field oriented parallel to the direction of propagation of the microwaves

The electrons (in resonance) orbit in the direction of the magnetic field and thus have a very long mean free path increasing the ionization probability and resulting in a higher density plasma source (orders of magnitude higher than in an RF only plasma)

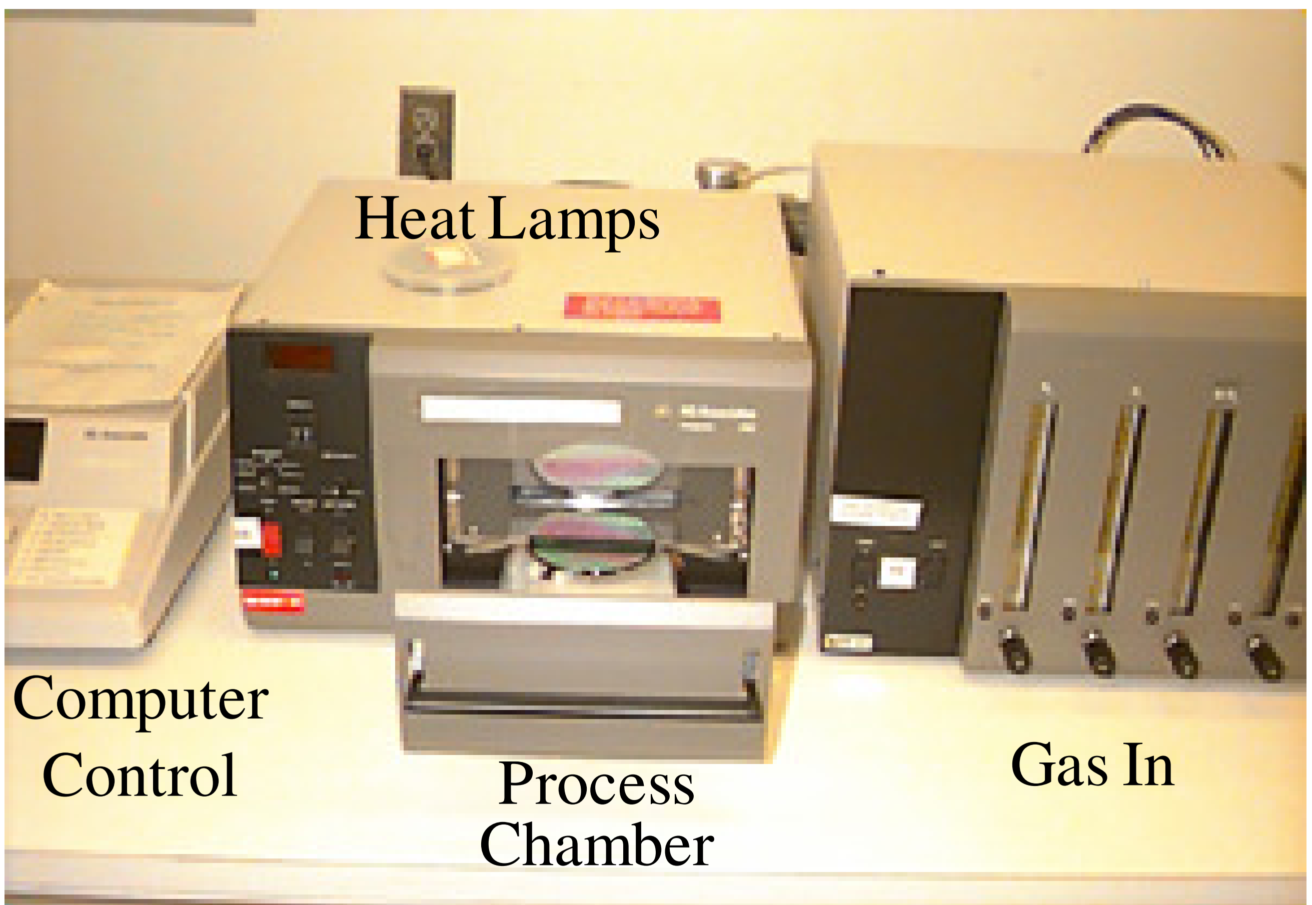
External RF bias is used to tailor the ion energy and flux

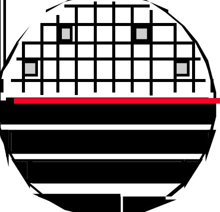


Solid State Technology, Nov. 1995



RAPID THERMAL PROCESSING (RTP)





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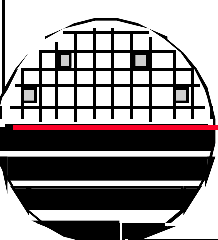
RADIANT HEATING EPI REACTOR



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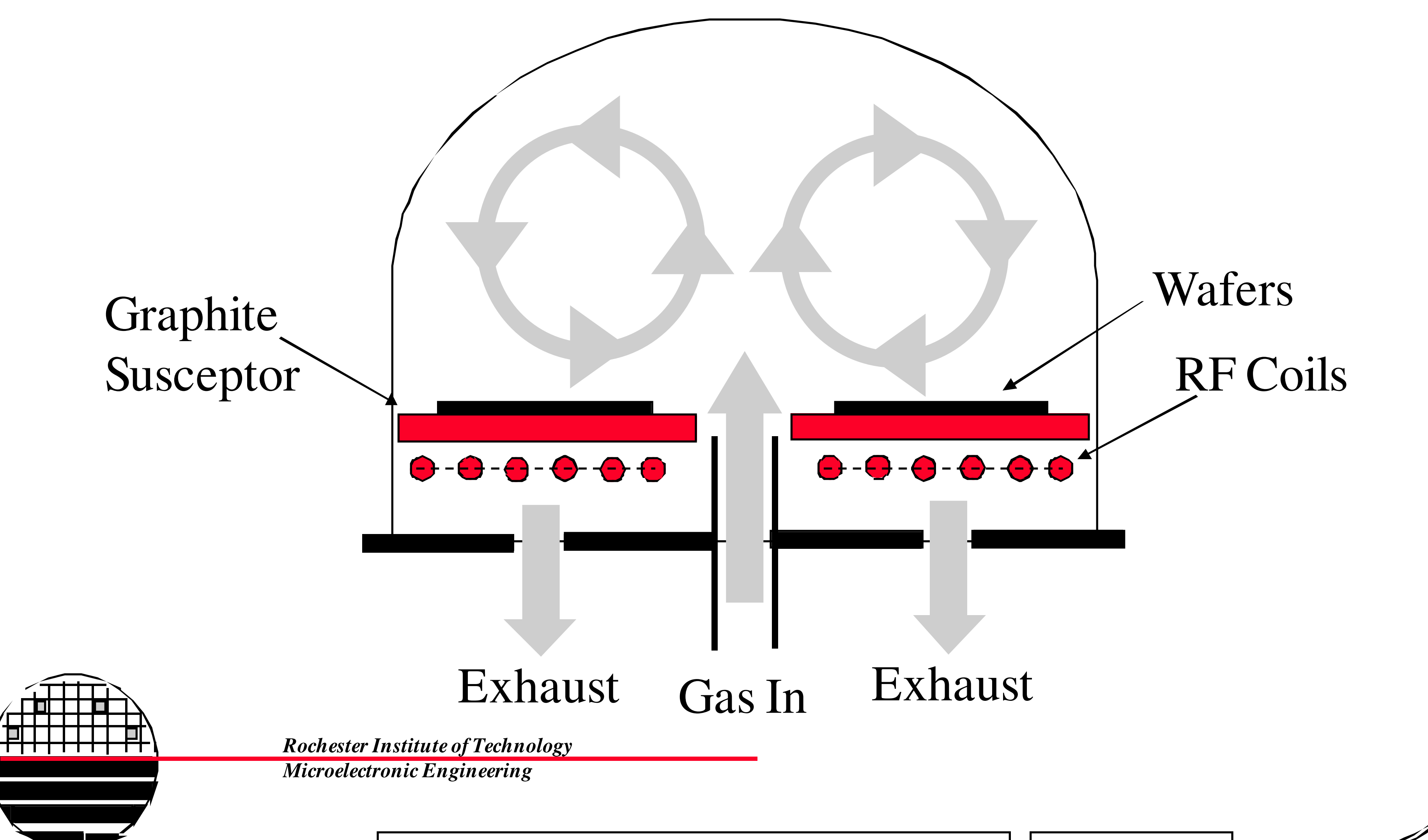
RADIO FREQUENCY HEATING (RF)



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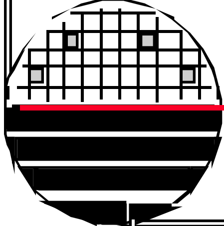
LPCVD EQUIPMENT

RIT's 6" and 4" LPCVD Systems



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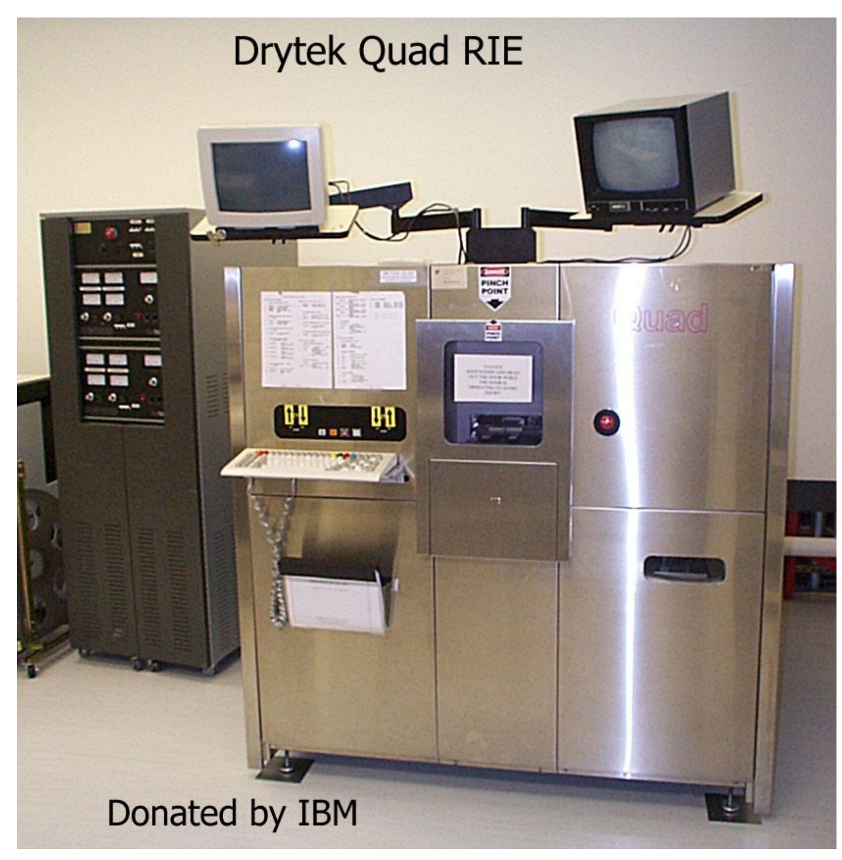
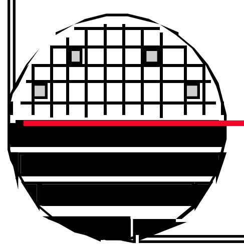
PECVD OF CARBON FILM (DIAMOND LIKE FILM)

Drytech Quad Tool – Chamber 4
CH_4 flow 45 sccm +/- 40%
50 mTorr +/- 10%
200 Watt +/- 50%
Deposition Rate ~ 300 Å/min
Index of Refraction = 1.8



Etch Rate:

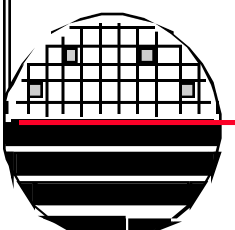
In KOH = ~ 0
In BHF = ~ 0
In Oxygen Plasma = fast



Ellipsometer Measurement
Pattern 20 Program 26 to find Index NU
Pattern 20 Program 21 to find Thickness TU

SAFETY CONSIDERATIONS FOR CVD

Toxic, Flammable gas is stored in exhausted gas cabinets, each with sprinkler and gas leak detector. The bottles have small diameter (0.010”) orafice to limit gas flow from the tank in case of a broken distribution line.



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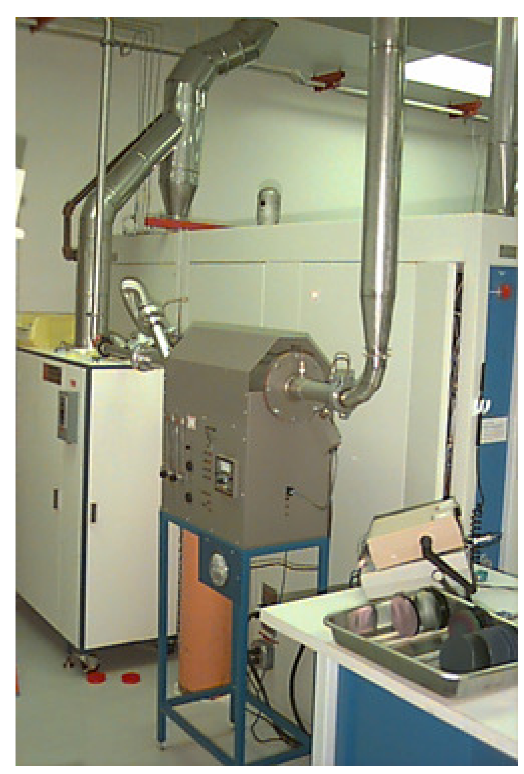
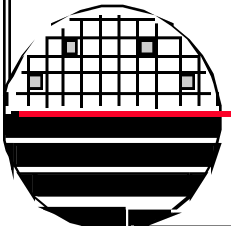
BURN BOX

The correct name is controlled combustion/reaction system. Exhaust gas exits through the "burn box" which is heated to 850 °C. At this temperature the exhaust gas reacts with air and any material that can burn is burned under controlled conditions within the "burn box"





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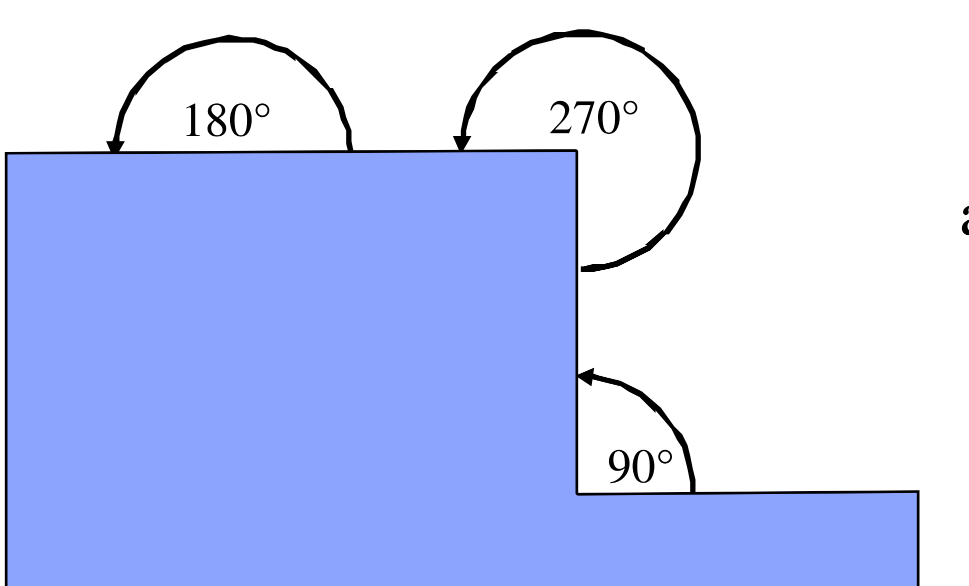
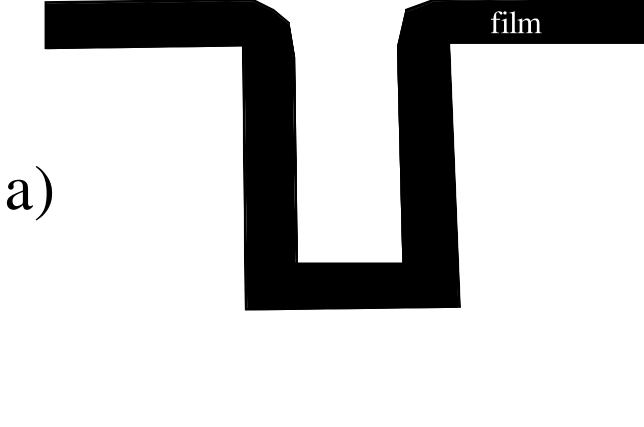
STEP COVERAGE WITH CVD FILMS

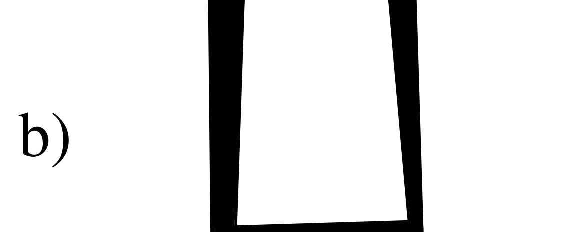


Deposition Rate is Proportional to Arrival Angle

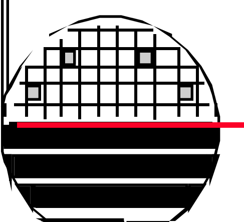
a)



b)



a) High surface migration rate conformal coating
b) Low surface migration rate



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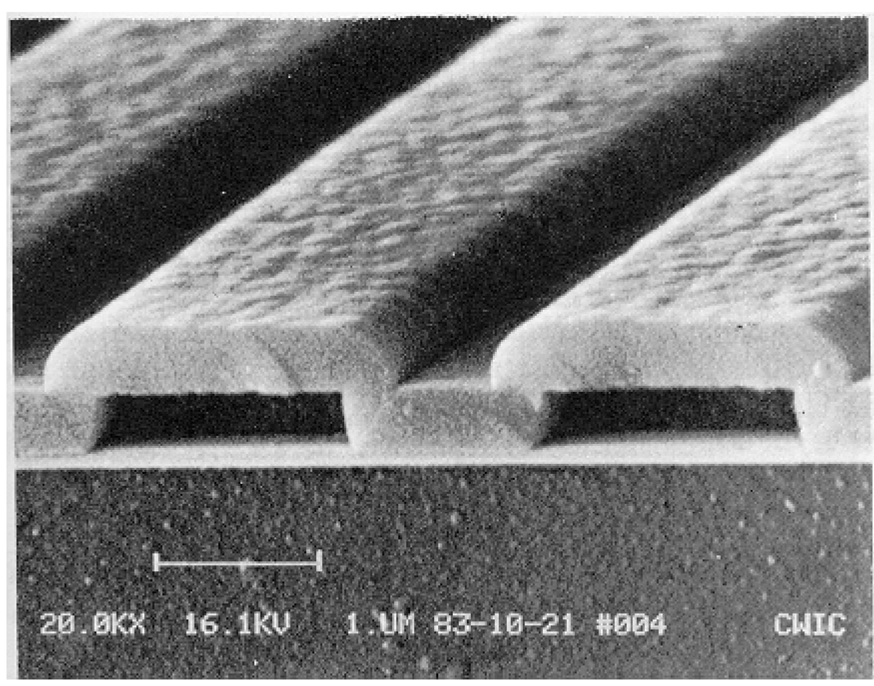
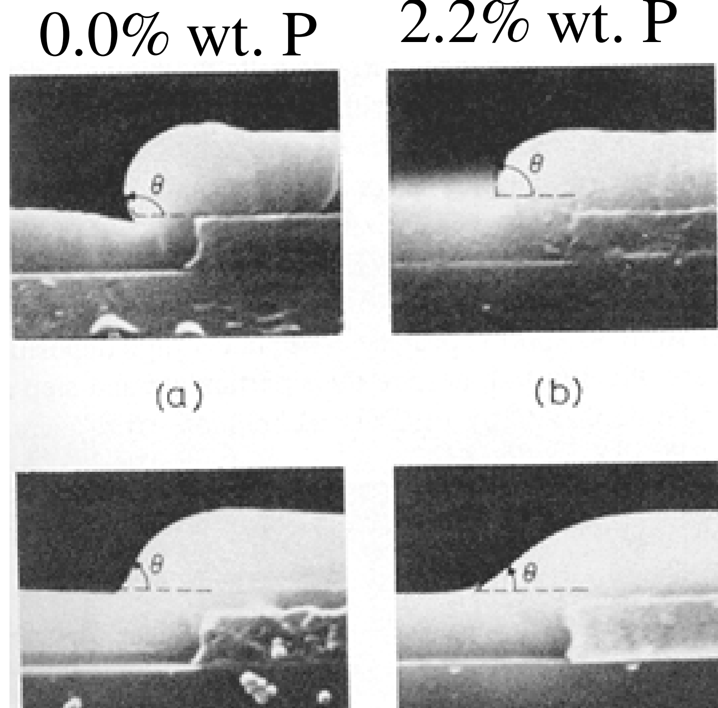
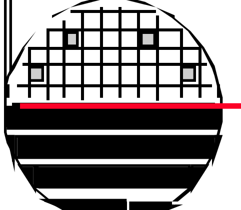
FLOW OF PHOSPHO/BORO/SILICATE GLASS



Conformal Coating



After anneal in steam at 1100 °C for 20 min



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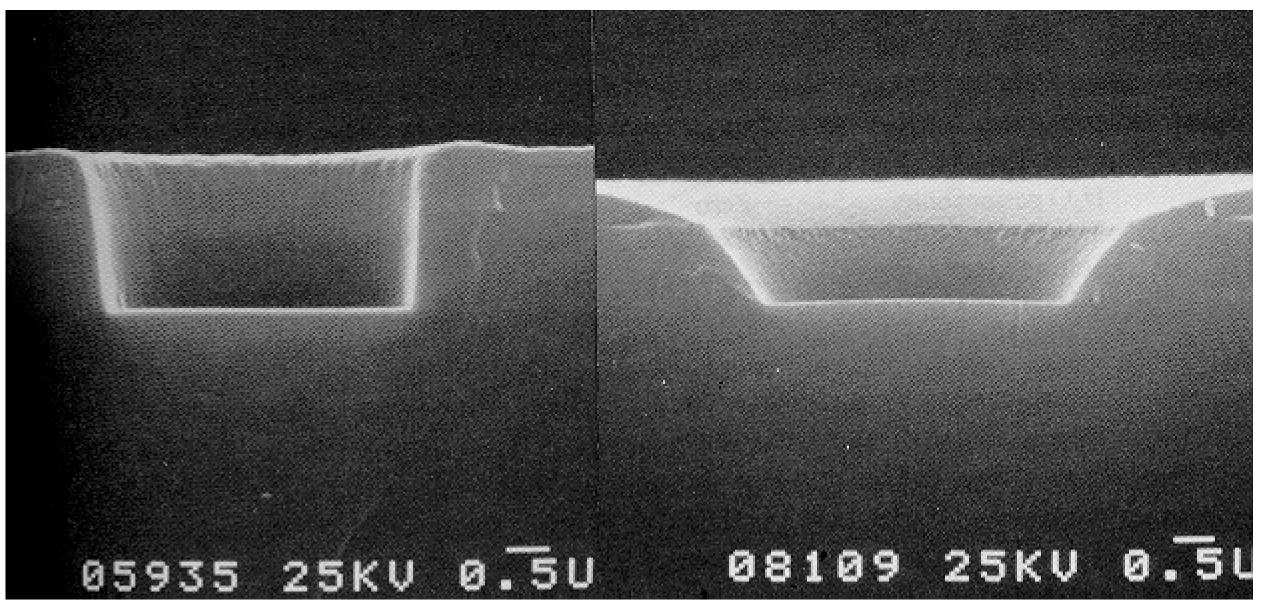
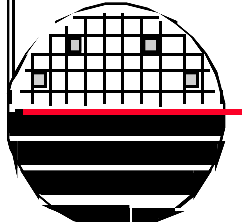
REFLOW OF BPSG



4 wt % P and 4 wt % B reflowed at 930 °C for 25 min.



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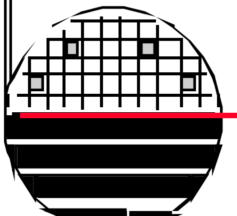
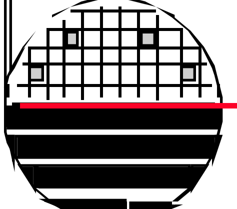
2. The Science and Engineering of Microelectronic Fabrication, Stephen A. Campbell, Oxford University Press, 1996.



HOMEWORK - CVD

1. Design a process to give a 1500 Å thick silicon nitride film.
2. Design a process to deposit a 6000 Å thick poly silicon film.
3. A particular process is reaction rate limited at 700 °C and the activation energy is 2 eV. At this temperature the deposition rate is 1000 Å/min. What would you expect the deposition rate to be at 800 °C? If the measured deposition rate at 800 °C is lower than expected what might the conclusion be? How would you prove it?



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