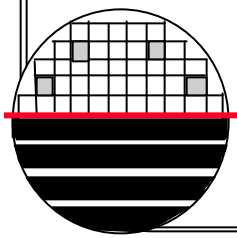
ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Reliability of Integrated Circuits and Semiconductor Devices

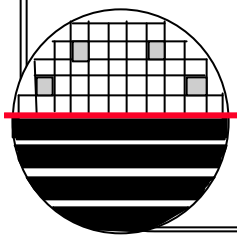
Dr. Lynn Fuller

Motorola Professor
Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041
LFFEEE@rit.edu
http://www.microe.rit.edu



OUTLINE

Introduction to Reliability
Accelerated Testing
Failure Mechanisms
Electrostatic Discharge
Alpha Particle Induced Soft Errors
Radiation Hard Devices
Aluminum Electromigration
Sodium Migration
Hot Electron Damage
Oxide Breakdown
Latch Up



INTRODUCTION TO RELIABILITY

Define a unit of failure rate as

1 Failure unit = 1 FIT = 1 failure/10^9 device hrs

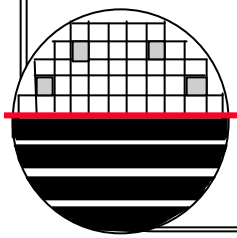
Example: System with 100,000 discrete parts, has one failure per month, then the failure rate

λ = 1 failure / 100,000/(30x24 hrs) = 14 E -9 = 14 FIT

Summary:

FIT	Failures/month	# devices failing in 10 years
10	0.7	0.1%
100	7	1.0%
1000	70	10%

A failure rate of <10 FIT is needed. At 1000 FIT there are about 2 failures/day and the entire system will be replaced over its lifetime



INTRODUCTION TO RELIABILITY

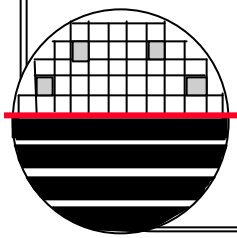
Testing Reliability and Proving Reliability is Time Consuming and Expensive as Illustrated in These Tables

Table 1: For 100 devices on test

FIT	Test Time for 1 failure (Years)
10	114
100	11
1000	1

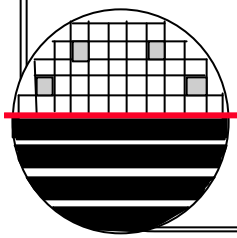
Table 2: For 500 devices on test for 6 months and no failure, then there is a Confidence Level that FIT is >

60%	325
90%	430
95%	1400
99%	2100



INTRODUCTION TO RELIABILITY

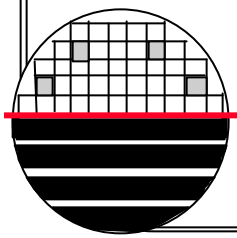
Testing is further complicated by the existence of more than one failure mechanism. Often one of the failure modes is characterized by a short median life and represents a small percentage of the total population, and represents the early failure mechanism. The remainder of the population has a longer median life and represents the steady-state failure mechanism. Burn in can find and eliminate the early failure devices.



MATHEMATICS OF FAILURE RATES

SEE SZE PG 614 TO 624

Cumulative Distribution Function
Reliability Function
Probability Density Function
Failure Rate
Mean Time to Failure
Exponential Distribution Function
Weibull Distribution Function
Log-Normal Distribution Function
Failure Populations

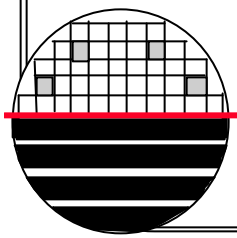


ACCELERATED TESTING

Stresses are used to accelerate failure. For example temperature cycling is used to accelerate mechanical failure.

- **Temperature Acceleration**
- **Voltage Acceleration**
- **Current Acceleration**
- **Humidity Acceleration**

Different failure mechanisms may be accelerated by different amounts for the same stress.



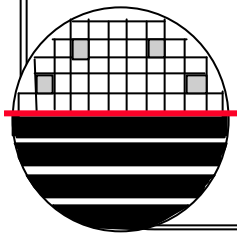
TEMPERATURE ACCELERATION

Temperature Acceleration can be used with many physical or chemical failure mechanisms. These mechanisms are often described by the Arrhenius Equation:

$$R = Ro \exp [Ea/KT]$$

where R is the Response, Ro is the pre exponential term, Ea is the activation energy in electron volts, K is Boltzman constant (8.6e-5 eV/K) and T is temperature in degrees absolute.

Plot the natural logarithm of the time to fail versus the inverse of the absolute temperature. The slope will give the activation energy.



TEMPERATURE ACCELERATION EXAMPLE

Example: 10% of metal lines fail due to electromigration failures in 200 hours at 175 C, in 32 hours at 200 C and in 4 hours at 250 C. Find the activation energy and pre exponential term, Ro. Plot the three points on ln(response) vs (1/T) plot.

Time for 10% failures = Ro exp[Ea/KT]

$200 = Ro \exp (Ea/K(273+175))$

$32 = Ro \exp (Ea/K(273+200))$ and K=8.6E-5 eV/K

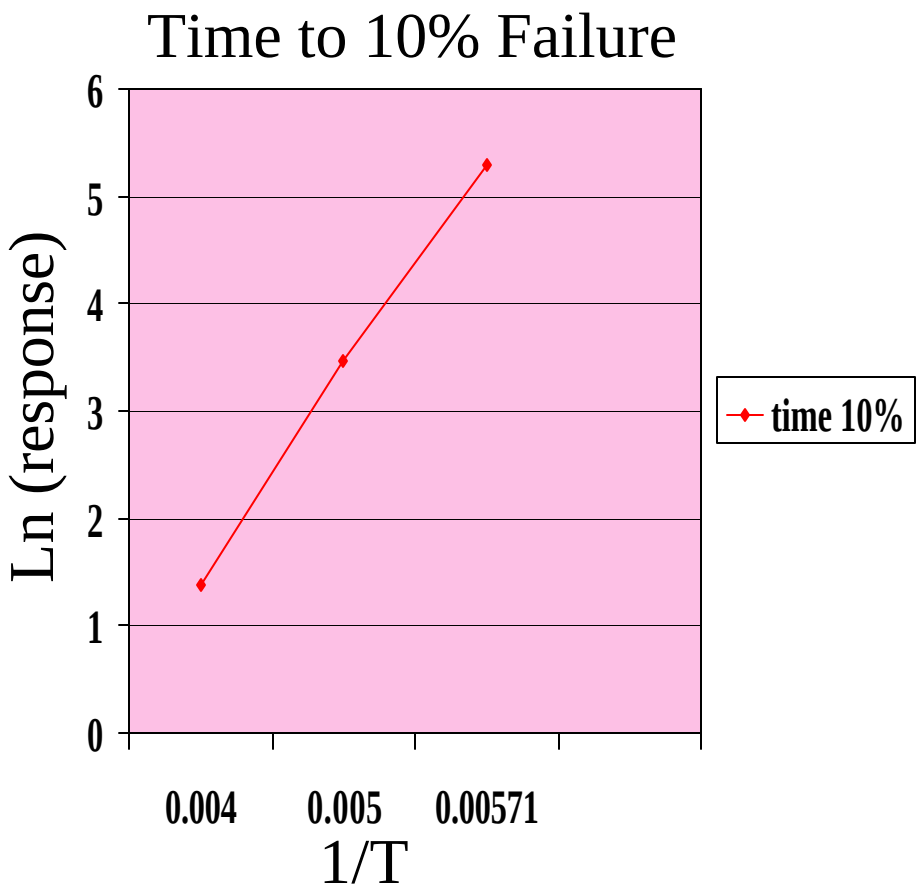
$$Ea = \frac{K \ln (200/32)}{(1/448 - 1/473)}$$

Ea = -1.34 eV and Ro = 3.86E29

TEMPERATURE ACCELERATION EXAMPLE

Slope = Ea/K

Since this plot is linear then we assume the response to exhibit Arrhenius Behavior

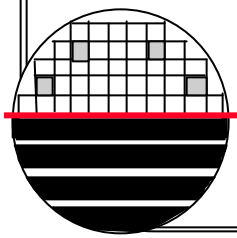


TEMPERATURE ACCELERATION

Acceleration Factor and Time Equivalent to 40 Years

	Acceleration Factor		Time Equivalent to 40 years in Hours	
Temp (°C)	Ea = 1.0 eV	Ea=0.5 eV	Ea=1.0 eV	Ea=0.5 eV
300	2.2e6	1500	0.2	233
250	3.2e5	570	1.1	616
200	3.1e4	176	11	2,000
150	1700	41	200	8,526
125	300	17	1,200	20,200
85	11.5	3.4	30,000`	103,000

Temp Ambient = 60 °C



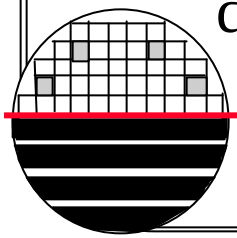
VOLTAGE AND CURRENT ACCELERATION

Most studies model voltage and current acceleration using voltage (or electric field) and current density raised to some power $\gamma(T)$ that is a function of temperature. $\gamma(T)$ usually has values between 1 and 5. Large increases in voltage can not be used because the integrated circuit will not function correctly but reliability measurements should be done at the extremes of allowed voltage.

$$R(T,V) = Ro(T)\, V^{\gamma(T)}$$

$$R(T,J) = Ro(T)\, J^{\gamma(T)}$$ where Ro(T) is a constant

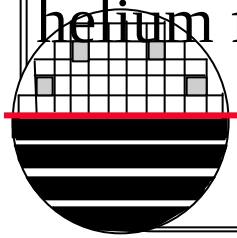
Increasing voltage can accelerate dielectric breakdown, accumulation of interface charge, and corrosion. Increasing current density accelerates electromigration.



HUMIDITY-TEMPERATURE ACCELERATION

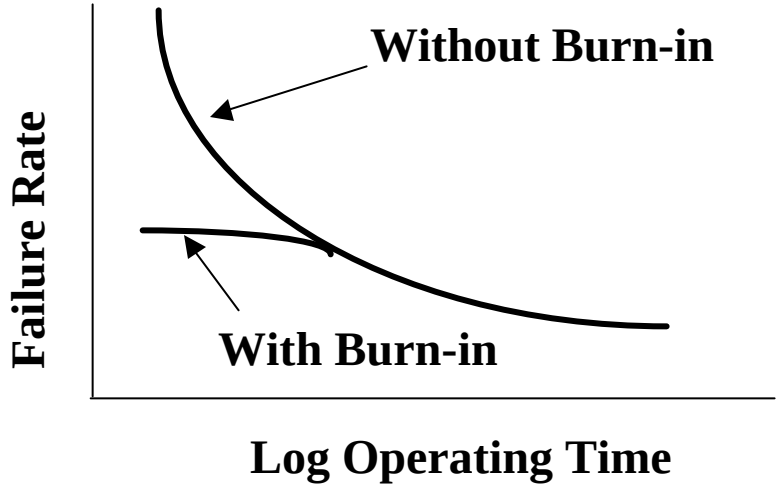
Hermetic packages prevent water from reaching the integrated circuit. Only metal and ceramic packages are hermetic. Plastic packages are much less expensive but will allow water to quickly penetrate to the integrated circuit. Humidity (water vapor) accelerates corrosion and can cause metallization failure.

Testing of the seal integrity of Hermetic packages are called leak tests. Packages are first tested for gross leaks by immersing in hot flouroinert liquids and looking for bubble escaping from the package as the gas inside expands due to the increase in temperature. If the package passes the gross leak test it is given the helium leak test. The packaged devices are placed in a chamber that can withstand 2000 psi. The chamber is evacuated then back filled with helium at 2000 psi. and left for 1 hour. Any leaking packages will be filled with helium. The packages are removed and placed in a chamber attached to a helium leak detector. As the leak detector pumps on the chamber it can detect helium from packages that have leaks.



BURN-IN

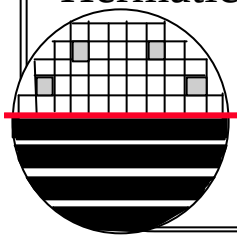
Burn-in is a technique to cause failure of parts that would fail early in its life prior to shipping the parts to the customer.



The devices are operated for some period of time during which most of the devices that are subject to infant mortality failure actually fail. Temperature cycling can also be used to eliminate infant mortality from weak wire bonds, cracks and other mechanical failure modes.

FAILURE MECHANISMS IN SILICON DEVICES

Device Association	Failure Mechanism	Relevant Factors	Accelerating Factors	Acceleration Activation Energy
Oxide and Interface	Surface Charge	Mobile Ions,V,T	T	Ea = 1.0-1.05
	Dielectric Breakdown	E,T	E,T	E^{γ},γ, (T) = 1- 4.4 Ea = 0.2 - 1.0 eV
	Charge Injection	E,T,Qf	E,T	Ea = 1.3 (trapping) Ea = 1.0 (hot electron)
Metal	Electromigration	T,J,A, gradients of T,J, grain size	T,J	Ea = 0.5-1.3 eV J^{γ},γ, (T) = 1- 4
	Corrosion	Contamination	H,V,T	
Bonds	Intermetallics	T, impurities	T	Ea = 1.0 - 1.05 eV
Hermaticity	Seal Leaks	Pressure	Pressure	



EXAMPLES OF FAILURE MECHANISMS

Electrostatic Discharge

Alpha-Particle-Induced Soft Errors

Radiation Hard Devices

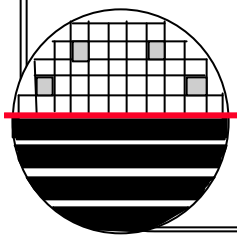
Metal Electromigration

Sodium Metal Migration in Gate Oxide

Hot Electrons

Oxide Breakdown

Latch Up in CMOS Circuits

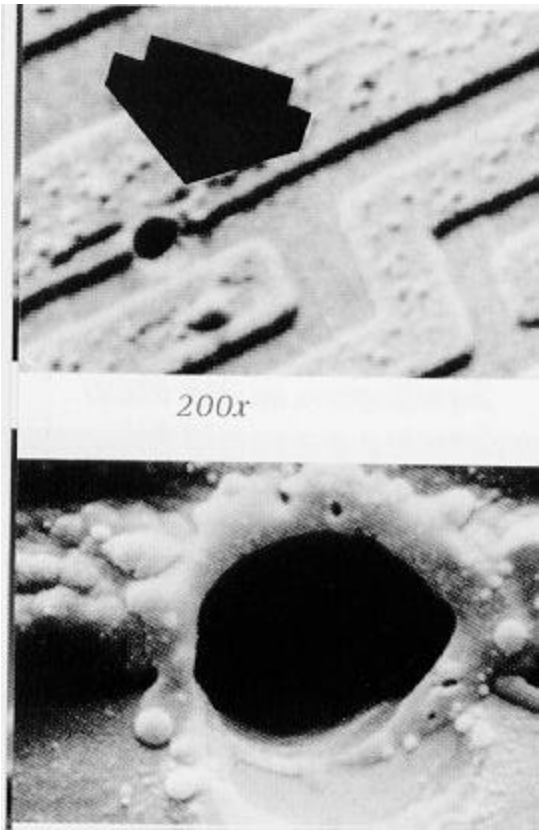


ELECTROSTATIC DISCHARGE

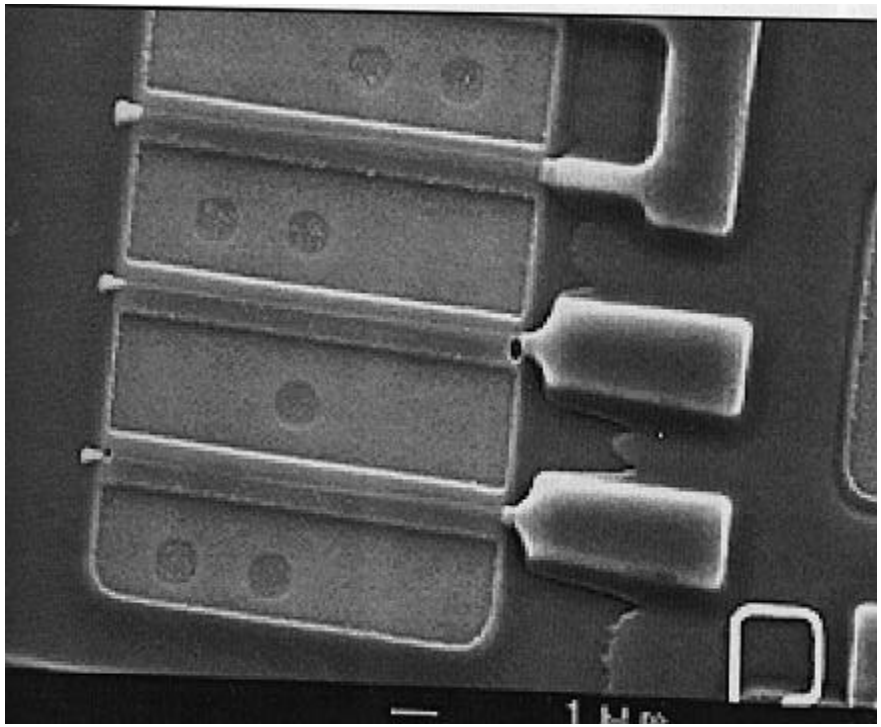
Electrostatic Discharge (ESD)

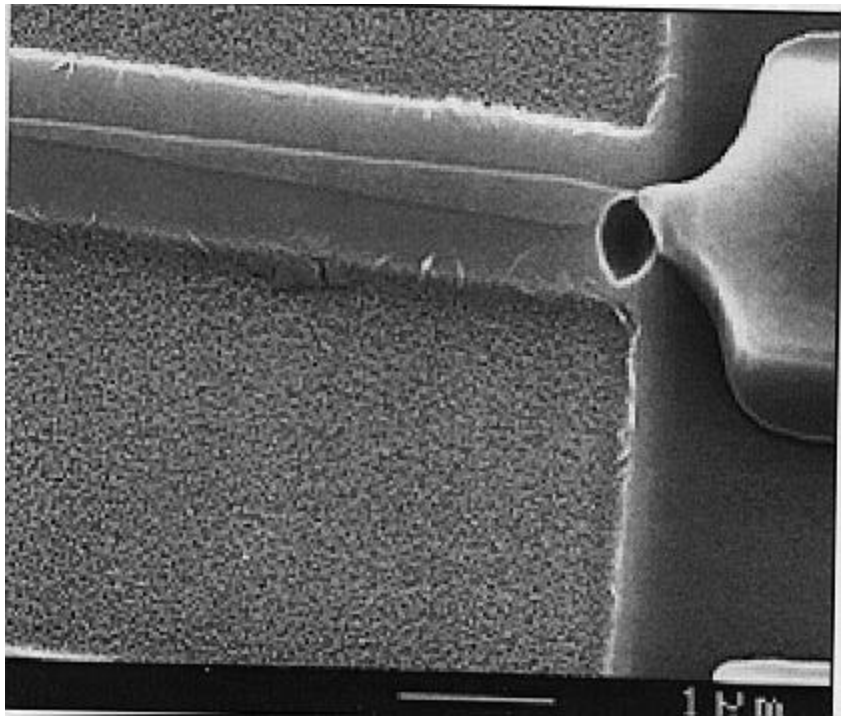
Dielectric Breakdown Strength of SiO2 is approximately 8 E6 V/cm, thus a 250 Å gate oxide will not sustain voltages in excess of 20 V

Triboelectricity (electricity produced by rubbing two materials together) can generate high voltages. A person walking across a room can generate 20,000 Volts and if discharged into an IC can cause immediate failure or damage that will reduce operating life. Even with proper handling several hundred volts can be applied to the IC. Therefore, protection circuitry is needed to provide a safe path for discharge of this electricity.

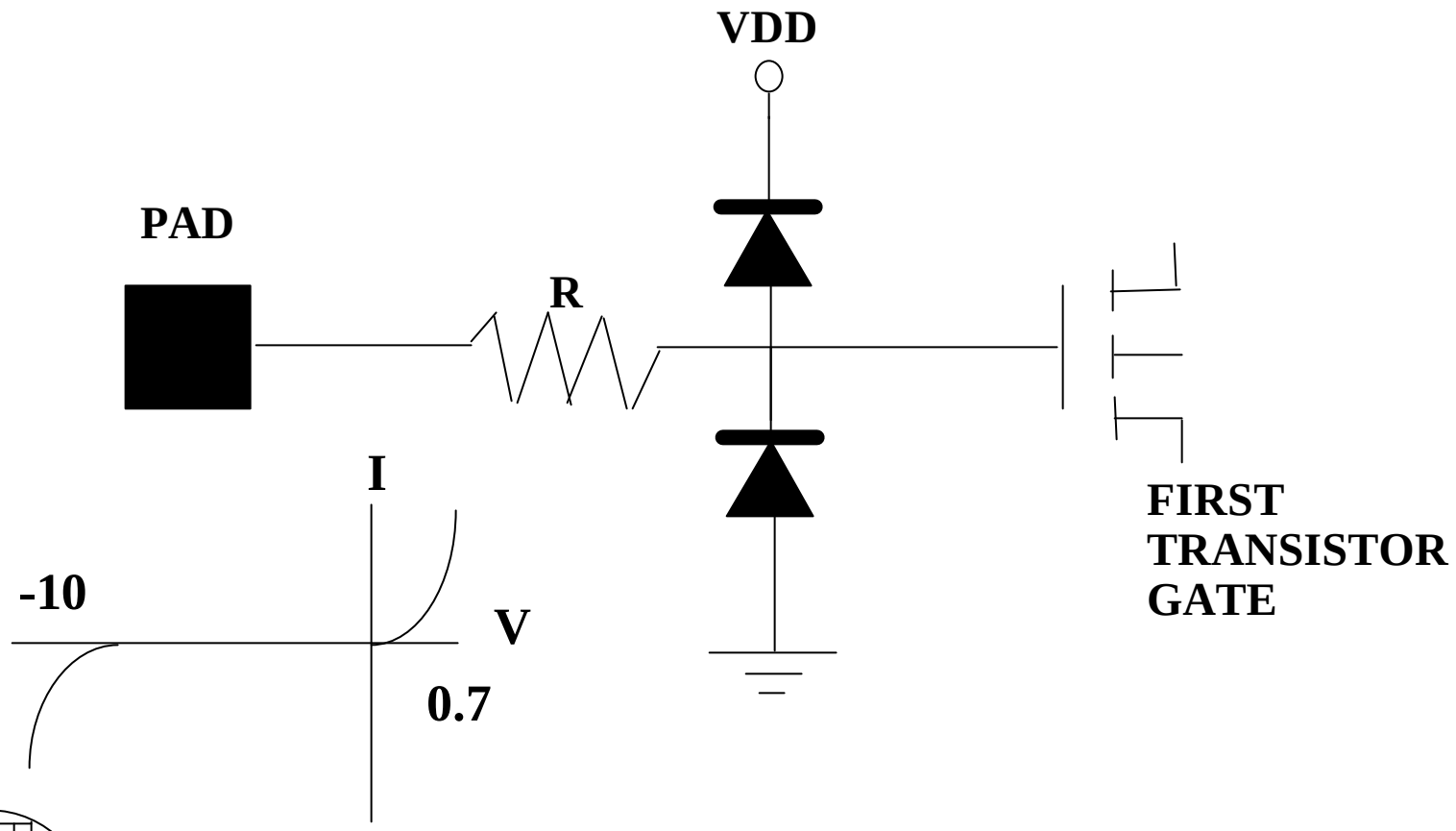


ESD DAMAGE



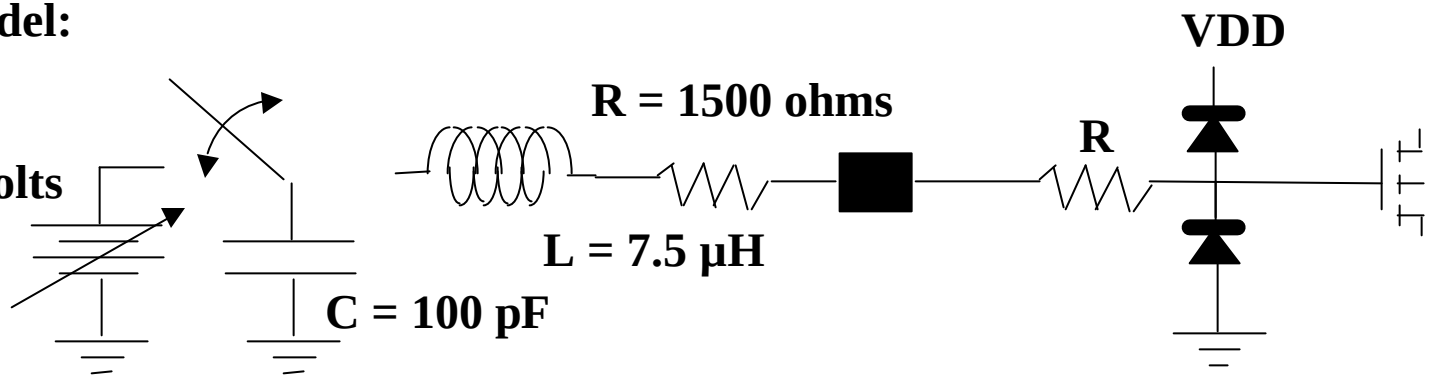


ELECTROSTATIC DISCHARGE - PROTECTION CIRCUITRY

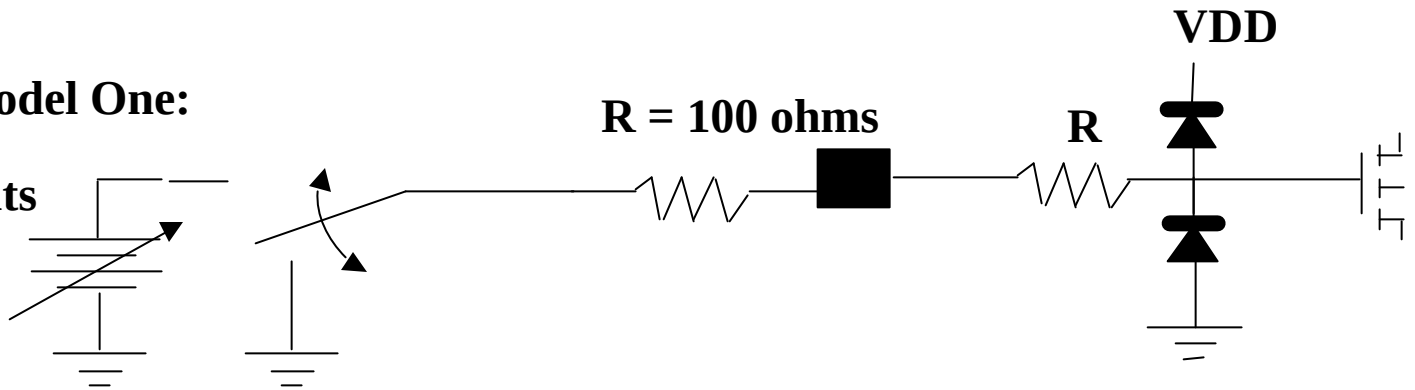


ELECTROSTATIC DISCHARGE - MODEL

Human Model:



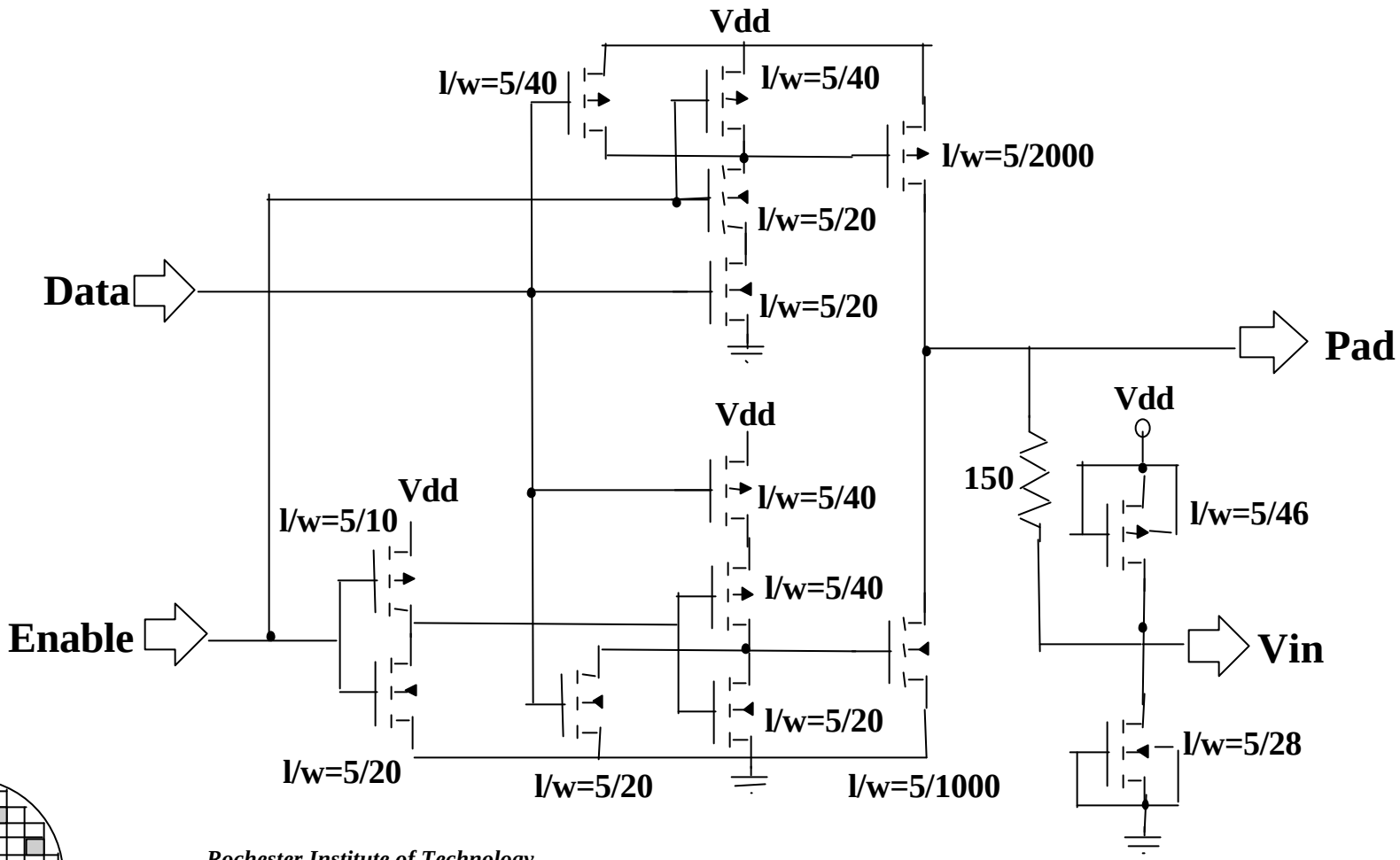
Machine Model One:



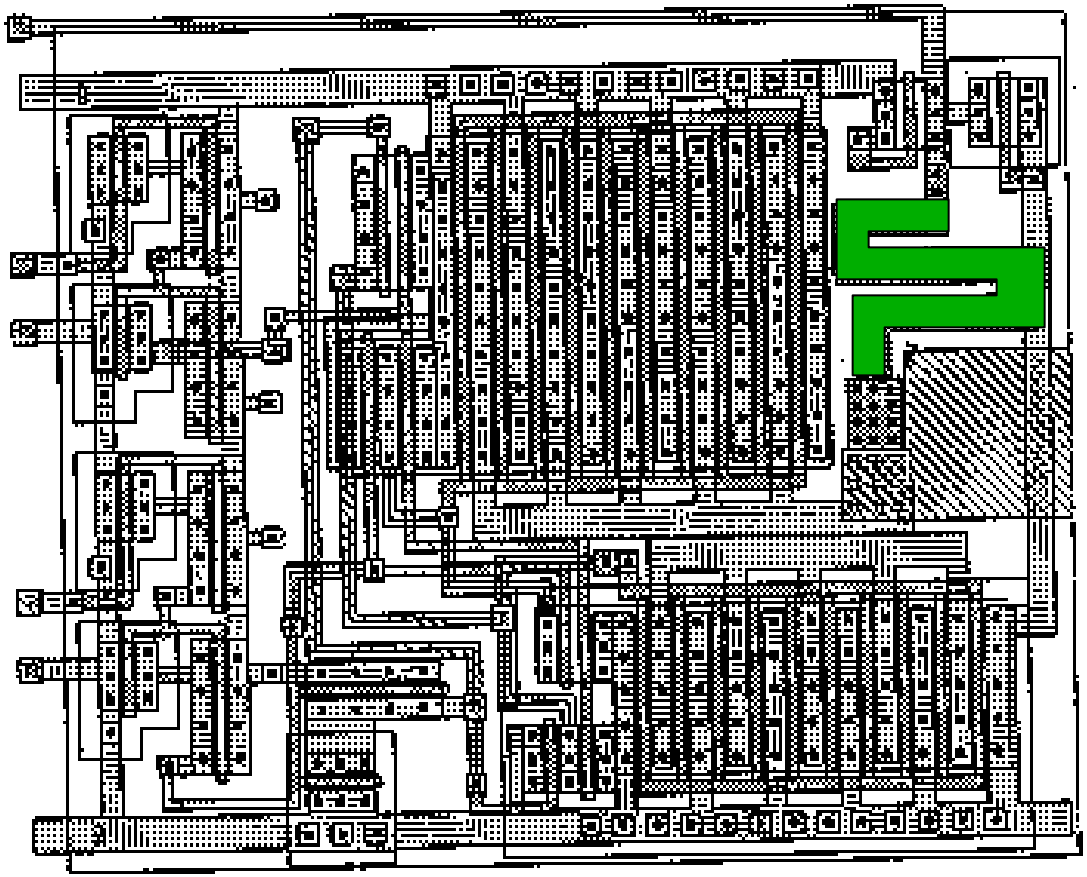
Machine Model Two
L = 1.0 µH
C = 200 pF
R = 10 ohms

Charged Device Model
L = 50 nH
C = 10 pF
R = 1 ohms

ELECTROSTATIC DISCHARGE - I/O PAD

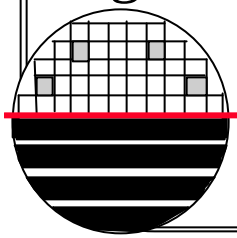


ELECTROSTATIC DISCHARGE - I/O PAD



ALPHA PARTICLE INDUCED SOFT ERRORS

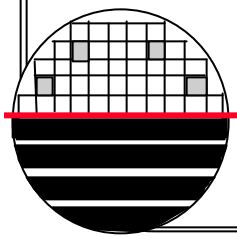
Radioactive elements, such as uranium or thorium, are naturally occurring impurities in IC packaging materials. The alpha particles emitted by these materials can cause soft errors in the ICs. The term "soft error" refers to a random failure not related to a physically defective device. The penetration of an alpha particle into the silicon causes the generation of an electron-hole plasma along the path of the particle. The generated carriers can cause the loss of information stored in the memory cells of a dynamic memory or stored in the depletion region of the drains of devices making up circuits such as dynamic shift registers or other logic units. The adsorption of a 4 MeV alpha particle can generate 10e6 electron hole pairs, which is equal to or greater than the charge stored in a dynamic memory cell.



ALPHA PARTICLE INDUCED SOFT ERRORS

To illustrate the seriousness of the problem, a typical soft error rate in a memory system containing 1000 16K memory devices may be on the order of one soft error per 1000 hour, corresponding to a device failure rate of 1000 FIT.

The incidence of soft errors can be reduced by surrounding or coating the IC chip with a material having a very low density of radioactive contamination. For example, alpha particles with an energy up to 8 MeV are completely absorbed in 50 μm of silicon rubber, and this material does not emit any significant amount of alpha particles



RADIATION HARD DEVICES

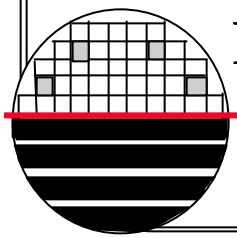
Military and Space Applications Need Radiation Hardened CMOS Integrated Circuits (See Harris Radiation Hard Data Book)

Radiation Damage Causes

- **Vt Shifts**
- **Reduced Mobility (lower gm)**
- **Degradation of Field Vt**
- **Latch-up**

Radiation Hardened Devices Use

- **SOS or SIMOX Technology**
- **Thin Gate Oxides, Shallow Devices**
- **n-MOS Rich Circuit Designs**
- **P-Well Technology with Guard Rings**

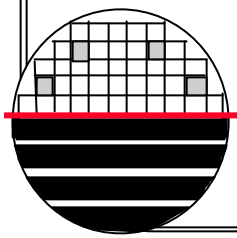


ALUMINUM ELECTROMIGRATION

Electromigration is the process whereby a flow of electrons moves aluminum atoms in the direction of the flow. Since these atoms are about 20,000 times heavier than electrons, they must be thermally activated and the current density must be high. High current density occurs wherever a thinning of the metal trace occurs, either a design error, step coverage problem, scratch, void or point defect. Larger grains are harder to move than fine grains and grain size is proportional to the film thickness. Covering the aluminum with a passivation layer can reduce electromigration by a factor of 10, using a 2 to 8% mixture of copper in the aluminum can reduce electromigration by another factor of ten.

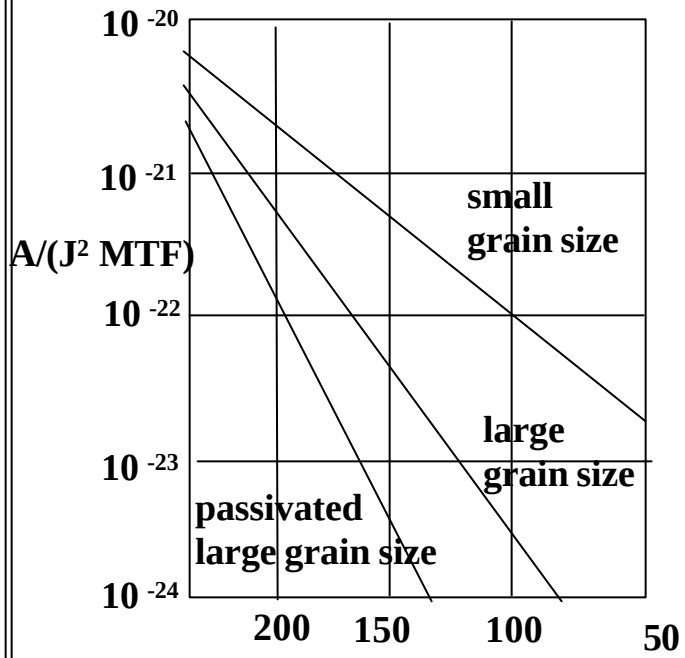
$$\mathbf{MTF = C\ Area/J^2\ \ exp\ -Ea/KT}$$

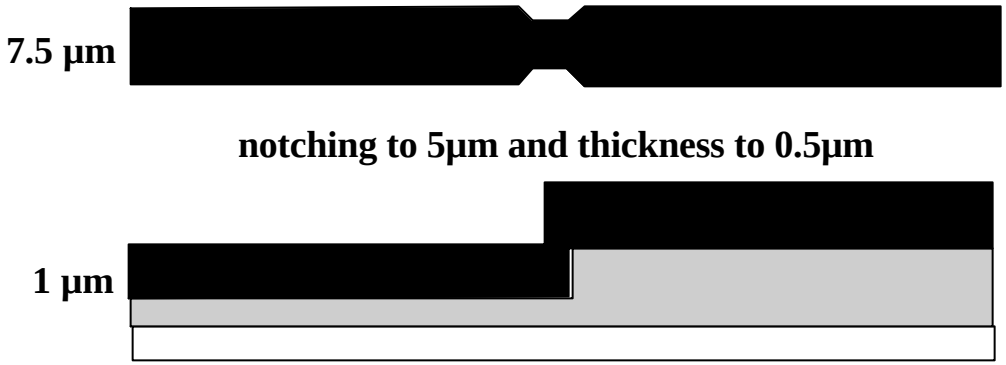
where C is a constant, J is Current Density, and Ea is the activation energy



ALUMINUM ELECTROMIGRATION

Example: Determine the median time to failure caused by aluminum electromigration for nominal and worst case sections shown below when at 100mA dc current flow and 125 °C. Assume aluminum is large grain and not passivated.





$J = 1/A = 1.33 \times 10^4$ A/cm^2 (nominal)

$= 4 \times 10^4$ A/cm^2 (worst case)

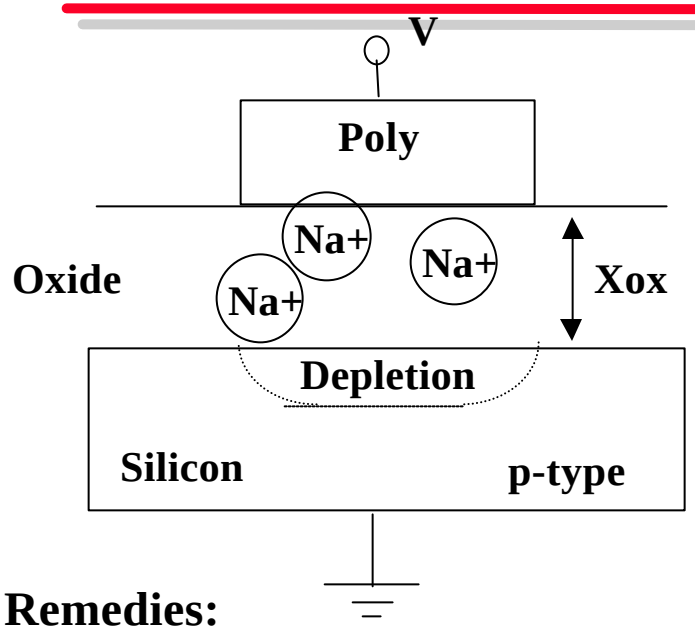
$A/(J^2\ MTF) = 1.2 \times 10^{-23}$

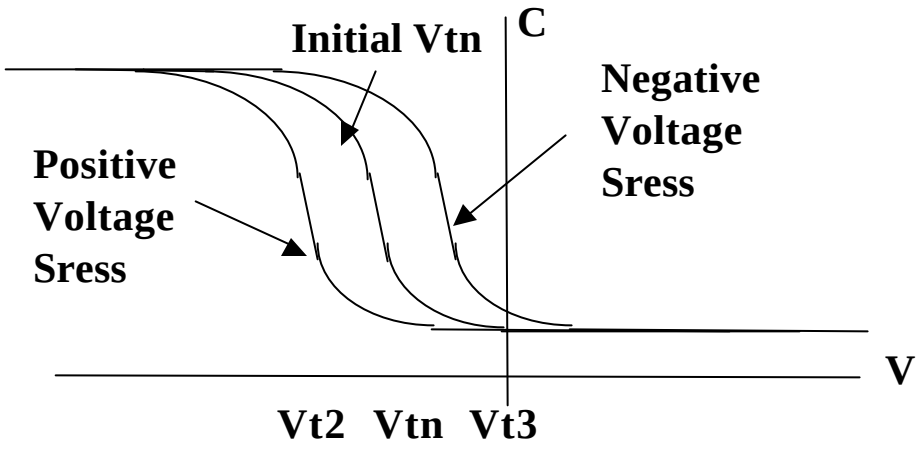
$MTF = Area/(J^2 \quad 1.2 \times 10^{-23})$

= 14,650 days with nominal conditions

= 542 days with worst case conditions

SODIUM MIGRATION



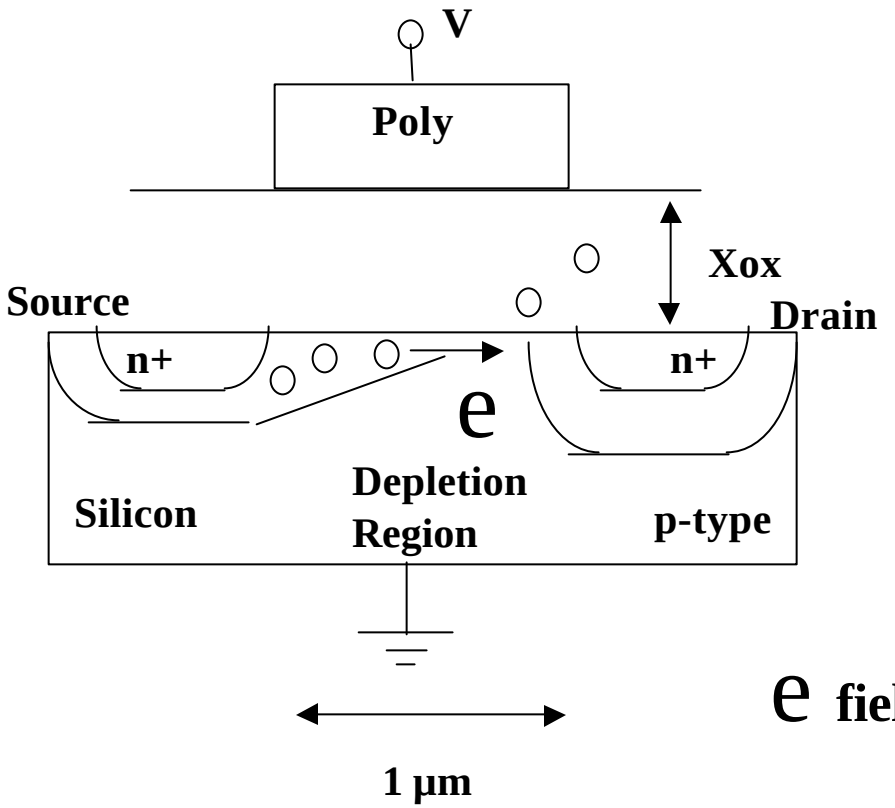


Remedies:

- Tube Cleaning in Acids
- Alumina Liners
- Steam Cleaning, wet N2
- HCl, TCA
- Double Wall Tubes

1. Measure Initial C-V Characteristics, Vtn
2. Bias at +20 Volts and Heat Substrate to 200 °C for 15 min.
3. Cool to 25 °C and Measure C-V, Vt2
4. Bias at -20 Volts and Heat Substrate to 200 °C for 15 min.
5. Cool to 25 °C and Measure C-V, Vt3
6. Voltage Shifts Greater than 0.3 Volts Indicate a Problem

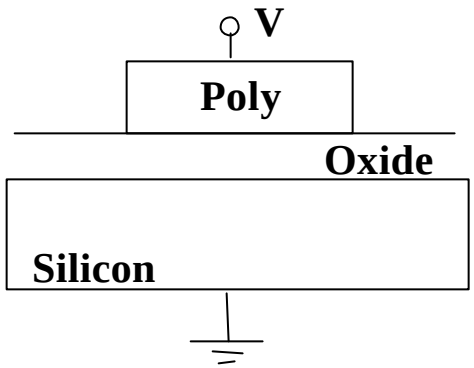
HOT ELECTRONS

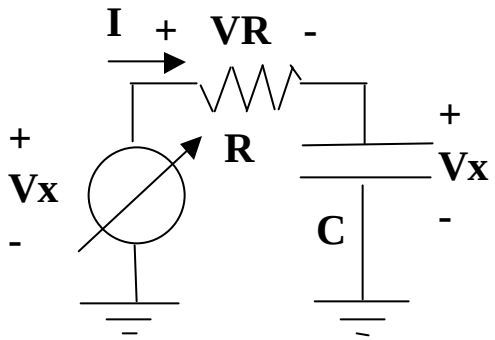


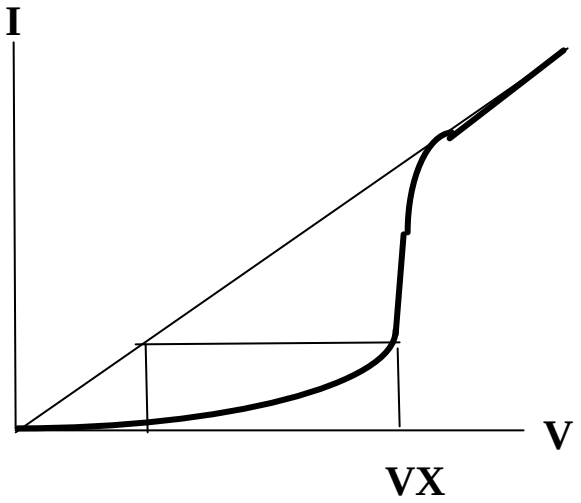
Electrons moving from source to drain are accelerated to high energy at the drain end of the MOSFET. These electrons can overcome the barrier and enter the oxide where they cause a shift in the threshold voltage.

e field = 1V / 0.1 µm = 1 x10^7 V/m

OXIDE BREAKDOWN

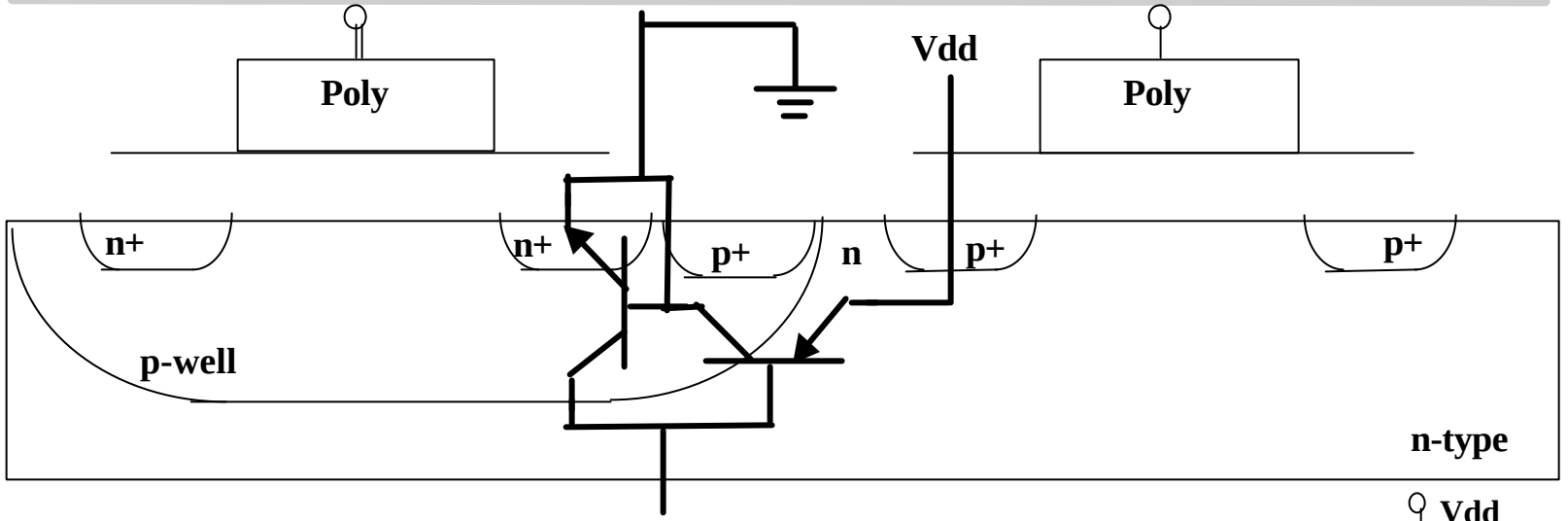






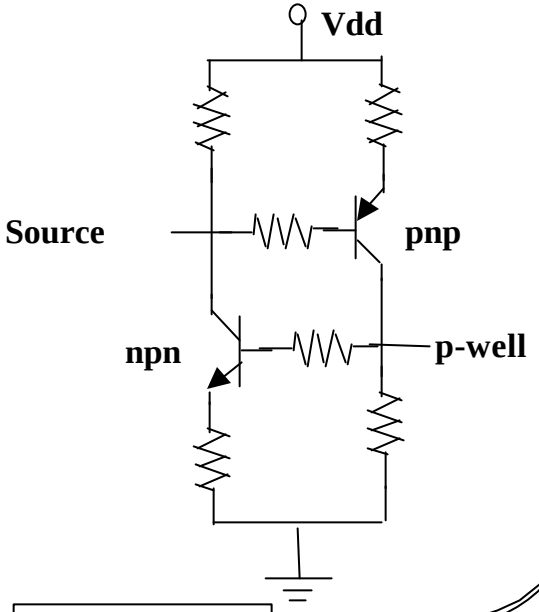
Breakdown Voltage = VX - VR

LATCH UP



The npn and the pnp transistor can both turn on creating a path between the supply voltage and ground. A disturbance such as electrons being injected into the substrate cause the pnp to turn on which in turn turns on the npn which causes the pnp to turn on, etc.

Remedies include increasing values of R's in the circuit or decreasing the current gain for the two BJT's

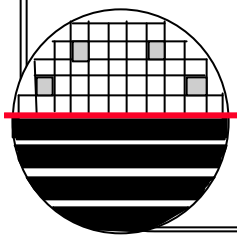


SUMMARY FOR RELIABILITY

The trend in modern VLSI technology will make the problems of maintaining high yield and high reliability more difficult.

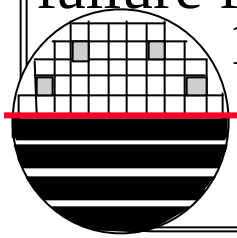
Small Dimensions
Higher Electric Fields, Larger Current Densities,
Larger chip size
Higher Power Dissipation, More Temperature Stress
More complex processes
New Materials Systems and New Failure Mechanisms

New Process Development must include identification and characterization of these failure mechanisms.



EXAMPLE

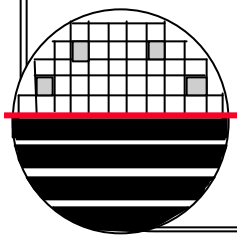
The gate oxide used in this CMOS process was studied through TDDB (Time Dependent Dielectric Breakdown) by aging large area (0.1 cm2) capacitors at 100 C and 150 C. Time to failure data were collected using both temperature and electric field as acceleration variables to characterize extrinsic and intrinsic failure modes. The extrinsic or defect mode is the primary source for oxide degradation on devices and results from localized weak spots induced from the manufacturing process. The intrinsic failure mechanism is related to the robustness of the technology and normally occurs well past the intended product live. Both linear (pessimistic) and reciprocal (optimistic) electric field acceleration models were used. The projected test structure extrinsic failure rates for 3.3 V and 80 C operation are 1 FIT for the linear model and <10- 4 FIT for the reciprocal model. Intrinsic oxide life was determined from measurements taken at 7 and 8 MV/cm and 150 C. Extrapolating to 3.3V and 80 C use conditions, the median time to failure for intrinsic life is 5.6E8 hours using the linear model and 1.1E16 hours using the reciprocal model.



REFERENCES

1. VLSI Technology, Ch. 14 - “Yield and Reliability”, Sze.

2. “Yield Analysis Software Solutions”, Semiconductor International, January 1996,Pg 79.



HOMEWORK - RELIABILITY

1. What is the definition of the FIT?
2. Calculate the voltage that corresponds to breakdown electric field for 150 Å SiO2 gate oxide.