ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

MCEE 550 CMOS IC Processing

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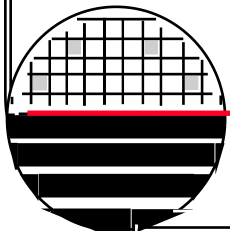

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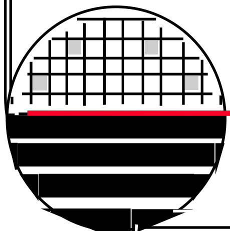

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INTRODUCTION

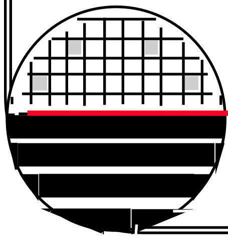
MCEE 550 CMOS IC Processing

Registration #MCEE-550

A lecture and laboratory course in which students design, manufacture and test CMOS integrated circuits. Topics include design of individual process operations and their integration into a complete manufacturing sequence. Students will be introduced to work-in-process tracking, ion implantation, oxidation , diffusion, plasma etch, LPCVD, and photolithography. Analog and digital CMOS devices will be designed, fabricated and tested.

Prerequisite MCEE-360, 502, 503, 505

Class 2, Lab. 6, Credit 4 Offered (Fall)



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MCEE 550 COURSE DETAILS

MCEE 550 CMOS IC Processing

Prerequisites: MCEE 360, 502, 503, 505

Course Goals: Design circuits and devices. Process silicon wafers through an entire CMOS process. Design unit processes and integrate into a complete process. Evaluate the process steps with calculations, simulations and lot history. Test completed devices.

Format: Lectures two times per week followed by laboratory two times per week. The laboratory starts with a discussion of current lot status and daily lab assignment.

Meeting Days: T,R 8:00am – 9:00am Room GLE-2030
Lab Time: lab twice per week for 3 hours, T,R 9:00am – 12noon

Grade:

Weekly Assignments	20%
Process Improvement Project	20%
Attendance	20%
Laboratory Notebook	20%
Laboratory Work	20%

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INSTRUCTOR INFORMATION

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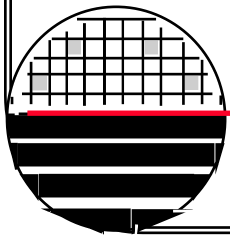
email:	SABEMCA@rit.edu
Tel	



MCEE 550 SCHEDULE

MCEE 550 CMOS IC Processing

Lesson No.	Discussion Topic	Lecture Document	Presentation, Excel References or Video	Homework
1.	Factory Orientation	out_550.pdf CMOS_Factory.ppt	Factory Presentation	HW on Factory
2.	Intro to Mesa	MESA.pdf	MESA Presentation	HW on MESA
3.	RIT's Submicron CMOS Process	SubCmos2014.pdf	Sub-CMOS Presentation	
4.	RIT's Submicron CMOS Process	SubCmos2014.pdf		
5.	RIT's Submicron CMOS Process	SubCmos2014.pdf		HW on Sub-CMOS
6.	TQM, SPC and Process Capability Analysis	TQM.pdf	TQM Presentation	HW TQM
7.	Adv MOSFET Basics	ADV_MOSFET_Basics.pdf		HW on Basics
8.	Advanced CMOS Technology Parts 1 & 2	ADV_CMOS_Part1-2.pdf		
9.	Advanced CMOS Technology Parts 1 & 2	ADV_CMOS_Part1-2.pdf		HW on Part 1 & 2
10.	Advanced CMOS Technology Part 3	ADV_CMOS_Part3.pdf		HW on Part 3
11.	ASML Stepper	ALIGN ASML.pdf		HW on ASML
12.	Ion Implant	implant.ppt	Implant Presentation	HW on Implant
13.	RIT's Advanced CMOS Process	AdvCMOS2012.pdf		
14.	RIT's Advanced CMOS Process	AdvCMOS2012.pdf		HW Adv-CMOS
15.	Wet Etch and CMP	wet_etch.pdf lec_cmp.pdf		HW on Wet Etch
16.	Particle Count Studies	par count.pdf		HW none

MCEE 550 SCHEDULE

17.	Testing Device Problem Analysis	Device-Problem-Analysis.pdf		HW none
18.	Testing	cmostest.ppt TestResults.ppt test_dig.ppt Test Manual CMOS TestingJohnGalt1.pdf NMOS_TEST_DATA.xls PMOS_TEST_DATA.xls		HW TBA
19.	Introduction to SPICE	Intro_to_LTSPICE.pdf MODELS for LTSPICE	Intro to LTSPICE Intro to LTSPICE.wmv	HW on Intro to LTSPICE
20.	Introduction to VLSI	IntroVLSI.pdf		
21.	Introduction to VLSI	IntroVLSI.pdf		HW on Intro to VLSI
22.	VLSI CAD	VLSI-CAD.pdf		HW on VLSI CAD
23.	SPICE MOSFET Models	SPICE.pdf SPICE Parameter Calc.XLS MODELS.txt		HW on SPICE
24.	SPICE Examples	SPICE Examples.pdf	SPICE_Examples	HW on SPICE Examples
25.	Microcontrollers	Microcontrollers.htm	Arduino Sensor.wmv	none
26.	Thanksgiving Break			
27.	DRAM	lec_DRAM.pdf		
28.	EEPROM	EEPROM.pdf		
29.	TBA			
30.	Reading Day			
31.	Final Exam or Presentation of Process Improvement Projects	Factory Projects.pdf		

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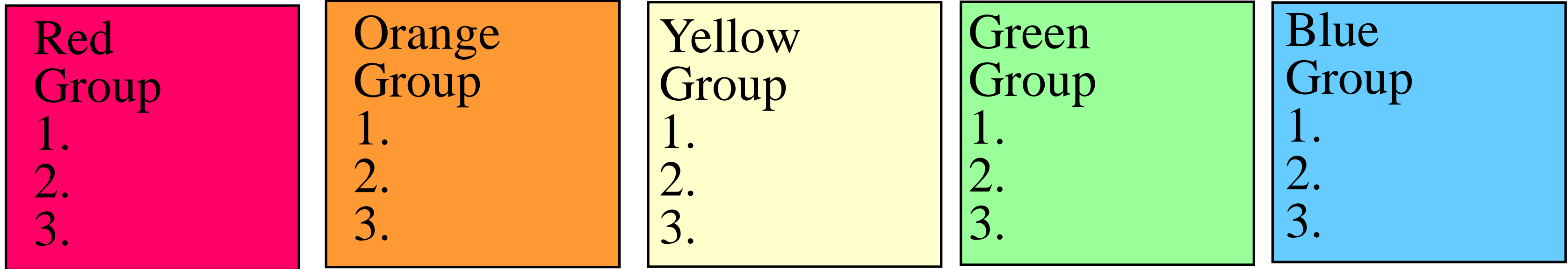
FACTORY (MULTIDISCIPLINARY) TEAMS

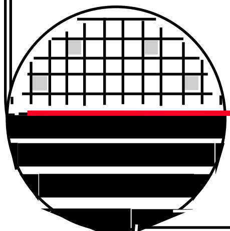


Every two weeks groups shift discipline (to the right). For example the red group does Diffusion week 1&2, Red does Lithography week 3&4, Red does CVD/Plasma week 5&6, etc.

Discipline

Diffusion	Lithography	PVD/Plasma Etch	CVD/PECVD	Wet Etch/CMP
Bruce Furnace	Canon Stepper	CVC601	ASM 6"LPCVD	Al Wet Etch
AG-RTP	SSI Track	Drytech Quad	P-5000	BOE Etch
Blue M Oven	CD Linewidth	Lam490	Nanospec	RCA Clean
Nanospec	Overlay	Lam4600	Spectromap	Hot Phos Nitride Etch
Spectromap	Branson Asher	Nanospec	Varian 350D	BOE
CDE Resistivity Map		Tencore P2		Solvent Strip
				CMP and CMP Clean
				Nanospec
				Surfscan
				SEM

While in each discipline the students will
- Process lots requiring steps in that discipline
- Perform follow up Inspection and Metrology
- Investigate and Update SPC data
- Monitor non-device process metrics
- Perform a "pass down" at the end of (2 weeks)
- Track lots in and out of Mesa



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FACTORY (MULTIDISCIPLINARY) TEAMS

Red Group	Orange Group	Yellow Group	Green Group	Blue Group
1. Jackson	1. Henry	1. Timothy	1. Wilkie	1. Spencer
2.	2.	2.	2.	2.
3.	3.	3.	3.	3.

Every two weeks groups shift discipline (to the right). For example the red group does Diffusion week 1&2, Red does Lithography week 3&4, Red does CVD/Plasma week 5&6, etc.

Discipline

Diffusion	Lithography	PVD/Plasma Etch	CVD/PECVD	Wet Etch/CMP
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AG-RTP	SSI Track	Drytech Quad	P-5000	BOE Etch
Blue M Oven	CD Linewidth	Lam490	Nanospec	RCA Clean
Nanospec	Overlay	Lam4600	Spectromap	Hot Phos Nitride Etch
Spectromap	Branson Asher	Nanospec	Varian 350D	BOE
CDE Resistivity Map		Tencore P2		Solvent Strip
				CMP and CMP Clean
				Nanospec
				Surfscan
				SEM

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- Process lots requiring steps in that discipline
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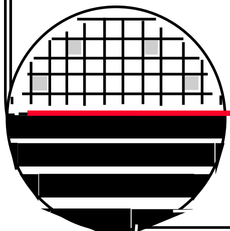
8-17-2014



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EXAMPLE SHORT LOOP PROCESS VERIFICATION RUNS

If no factory lots are available in a specific discipline then group will do short loop process verification runs:

BOE – Etch rate verification
RTP – Tool operation and recipe verification for TiSi and TiSi2 formation
PECVD – Tool operation and deposition rate verification for TEOS Oxide and Nitride
Resist Coat Thickness Measurement using Spectromap for Coat.rcp and CoatMtl.rcp Recipes used by Factory
Or

SPC Chart verification, evaluation and process capability improvement

Verify all MESA picture documents are correct

Verify MESA instructions are correct

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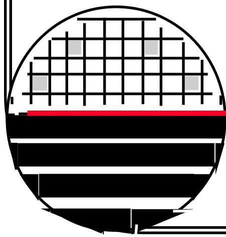
EXAMPLE PASSDOWN AT END OF ROTATION

Discipline: Lithography **Date:** Nov 30- Dec 9, 2014
Group Members: Matt McQuillan, Dave Pawlik

Lot Advancement:

F031013 – CC Photo –Changed Stepper Job to Align using TVPA Marks Only
added 2 µm shift to alignment key locations on pg 4/ in process file
F040119 – Resist Strip
F040614 – Active Photo
F031013 – LDDP Photo
F040920 – Resist Strip-Changed Stepper Job to Align using TVPA Marks Only
F040920 – P-Well Photo-Changed Stepper Job to Align using TVPA Marks Only
F030922- Resist Strip

Other: Short Loop Resist Coat Thickness measurement for Coat.rcp, Xpr=1.0 µm
Branson Asher often gives purge timeout error, select continue



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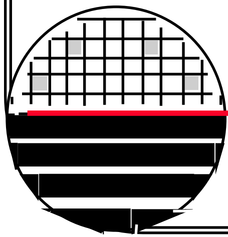
PROCESS IMPROVEMENT PRESENTATION

Each student will propose and carry out a design for improving the RIT CMOS process. Students can work in teams of two or individually. Project examples might include a change in plasma etch chemistry or a change in a furnace recipe. The proposed benefit and experimental verification is given in an oral presentation to the class in place of a final exam.



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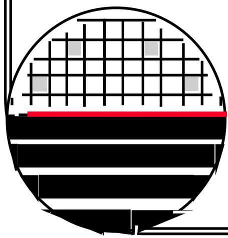
EXAMPLE PROCESS IMPROVEMENT PROJECTS

Lance Barron –Simulation of Masking Thickness for Ion Implant
Dan Ghiocel – Creating Canon Stepper Jobs for SMFL-CMOS Process
William Hart – Verification of Salacide Process with Nitride Spacers
Tiffany Hoover – Using the Spectromap in Factory Processing
Jae Jun Hwang – Verification of Two Layer Metal Process Details
Dan Jaeger – Improved Photolithography at Metal Level
Adam James – Evaluation of STI Etch, Fill and CMP
Robin Joyce – SEM Analysis of Completed Factory Wafers
George Mulfinger – Short Loop Verification of Side Wall Spacer Etch
Mike Slocum – Improved Hot Phos Nitride Etch Process
Katherine Walker – Alternative Well Doping Strategy for Adv-CMOS
Patrick Warner –Incorporation of PECVD TEOS in Factory Processes
Eric Woodard – Improved Metal Etch



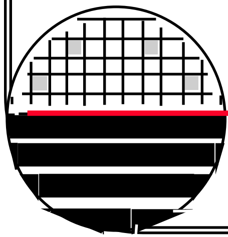
TEXTBOOK/REFERENCES

There is no required text for this course. You may wish to use the following textbooks as references. Purchase of lab notes (CD) is required.

1. Silicon Processing for the VLSI Era Volume I, S. Wolf and R.N. Tauber, Lattic Press, Sunset Beach, CA, 1986.

2. The Science and Engineering of Microelectronic Fabrication, S.A. Campbell, Oxford University Press, New York, NY, 1996.

3. VLSI Technology, Edited by S.M. Sze, McGraw-Hill Book Company, 1983.



HOMEWORK FORMAT GUIDLINES

1. At the top of the front page include the following information:

Rochester Institute of Technology — **Your Name**
Microelectronic Engineering — **Date**
MCEE 550- Assignment Description

2. Name/date/page number on each page
3. Use 8.5"x11" paper with clean straight edges (no spiral notebook paper)
4. Leave room on the left margin for 3 hole punch.
5. Staple pages with one staple in top left at 45°.
6. Use black ink, avoid color because it will not copy well.
7. Type
8. Computer simulations must consist of a summary page followed by the hard copies of the data with key results underlined or boxed.
9. No cover or title.
10. Homework is due 1 week after finishing the module. Late homework will be graded but may have the grade lowered.

LABORATORY NOTEBOOK GUIDELINES

The laboratory Notebook is an important tool. Each student will be required to have such a notebook.

Name, Date, Description on Cover
Notebook will be of the permanently bound type
Include Multidisciplinary Teams, CMOS Process listings (3), Product Layouts (4), Operator Certification Sheet
Include Process Improvement Notes.
Number each page
Sign and Date each page (witness signature)
Use a diary type format to take notes of what you do each day. Include enough details so that a reader can follow what you did.
Tape printouts, data tapes, etc. correctly into the notebook.
Use ink.
Be neat.

PROCESS IMPROVEMENT PROJECTS

Jackson –
Henry –
Timothy –
Wilkie –
Spencer –

- Fix all SPC Charts
- New Chip Designs
- CVC601 Pump Down Time
- 50A Gate Oxide Growth