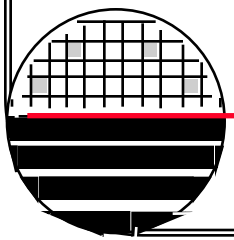
ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

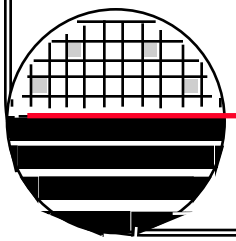
MCEE 732 Evaluation of Microelectronics Manufacturing

Dr. Lynn Fuller
webpage: http://people.rit.edu/lffeee
Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
email: Lynn.Fuller@rit.edu
microE webpage: http://www.microe.rit.edu



OUTLINE

Introduction
Course Details
Instructor Information
Lecture Schedule
Text/References
Contents of Lab Notebooks
HW Format Guidelines
Lab Notebook Guidelines
Lab Etiquette
Operator Certification



INTRODUCTION

MCEE 732 Evaluation of CMOS IC Processing
Registration #MCEE-550
MCEE-732 Evaluation of Microelectronic Manufacturing
This course focuses on CMOS manufacturing. Topics include CMOS process technology, work in progress tracking, CMOS calculations, process technology, long channel and short channel MOSFET, isolation technologies, back-end processing and packaging. Associated is a lab for on-campus section (01) and a graduate paper/case study for distance learning section (90). The laboratory for this course is the student-run factory. Topics include Lot tracking, query processing, data collection, lot history, cycle time, turns, CPK and statistical process control, measuring factory performance, factory modeling and scheduling, cycle time management, cost of ownership, defect reduction and yield enhancement, reliability, process modeling and RIT's advanced CMOS process. Silicon wafers are processed through an entire CMOS process and tested. Students design unit processes and integrate them into a complete process. Students evaluate the process steps with calculations, simulations and lot history, and test completed devices. (MCEE-601) Class 3, Lab 3, Credit 3 (S)

MCEE 732 COURSE DETAILS

MCEE 732 CMOS IC Processing

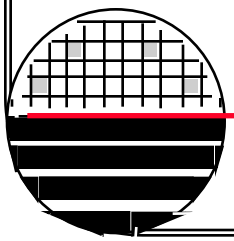
Prerequisites: MCEE 601

Course Goals: Process silicon wafers through an entire CMOS process. Design unit processes and integrate into a complete process. Evaluate the process steps with calculations, simulations and lot history. Test completed devices.

Format: Lectures three hours per week and laboratory one time per week. The laboratory starts with a discussion of current lot status and daily lab assignment.

Meeting Days: T,R 8:00am – 9:30am Room ENG-2510
Lab Time: lab once per week for 3 hours, Tuesday or Thursday 9:00am – 12noon

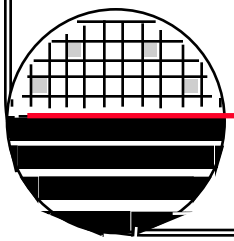
Grade:		
	Weekly Assignments	30%
	Attendance	20%
	Laboratory Notebook	20%
	Laboratory Work	30%



INSTRUCTOR INFORMATION

Name:	Dr. Lynn Fuller	**TA Name:**	Stephanie Bolster
email:	lffeee@rit.edu	**email:**	SABEMCA@rit.edu
Office	17-2553	**Office**	
RIT Tel	(585) 475-2035	**Tel**	
Home Tel	(585) 394-2949	**Fax**	
WebPage			

http://www.people.edu/lffeee



MCEE 732 SCHEDULE

MCEE 732 Microelectronics Manufacturing (Spring 2014)

Lesson No.	Discussion Topic	Reference Documents	Presentation or Video	Homework
1.	Factory Orientation Intro to Mesa	out_732.pdf CMOS_Factory.ppt MESA.pdf	Factory Presentation MESA Presentation	HW on Factory
2.	RIT's Submicron CMOS Process	CMOS2014.pdf	Sub-CMOS Presentation	HW on MESA
3.	RIT's Submicron CMOS Process	CMOS2014.pdf	Sub-CMOS Presentation	HW on Sub-CMOS
4.	TQM, SPC and Process Capability Analysis	TQM.pdf	TQM Presentation	HW TQM
5.	Review of IC Technology	REVIEW.pdf	Review Presentation	HW on Review
6.	Advanced MOSFET Basics	ADV_MOSFET_Basics.pdf		HW on Adv CMOS Basics
7.	Advanced CMOS Technology Parts 1 & 2	ADV_CMOS_Part 1-2.pdf		HW on Part 1 & 2
8.	Advanced CMOS Technology Part 3	ADV_CMOS_Part3.pdf		HW on Part 3
9.	ASML Stepper	ALIGN ASML.pdf		HW on ASML
10.	Ion Implant	Implant.pdf	Implant Presentation	HW on Implant
11.	CVD and RTP	CVD.pdf RTP.pdf		View Recipes at Labnotes
12.	Wet Etch Plasma Etch CMP	Wet_Etch.pdf Plasma Etch.pdf CMP.pdf		View Recipes at Labnotes
13.	Hand Calculations for Adv CMOS	HandcalcADV_CMOS.pdf		HW on Hand Calculations
14.	RIT's Advanced CMOS Process	AdvCMOS2012.pdf		
15.	RIT's Advanced CMOS Process	AdvCMOS2012.pdf		HW Adv-CMOS

MCEE 732 SCHEDULE

16.	0.25 µm CMOS Process Development	MAquilinoThesis.pdf VideoPresentation.ppt	Video File Available Upon Request	Watch the Video
17.	Defect Reduction and Yield Enhancement	lec_deft.pdf		HW on Wet Etch
18.	Particle Count Studies	par count.pdf bluebooties.pdf		HW none
19.	Factory Performance	fac_pfrm.pdf	Factory Performance	HW on Fac Performance
20.	Scheduling	lec_schl.pdf autosched.ppt input.xls	Factory Simulation	HW on Scheduleing
21.	Cycle Time Management	cycle.pdf CYCLE2MOD.XLS		HW on Cycle Time
22.	Reliability	lec_reli.pdf		HW on Reliability
23.	Testing Device Problem Analysis	Device-Problem-Analysis.pdf		HW none
24.	Testing	cmostest.ppt TestResults.ppt test_dig.ppt Test Manual CMOS TestingJohnGalt1.pdf NMOS_TEST_DATA.xls PMOS_TEST_DATA.xls		HW TBA
25.	Linear Technology LTSPICE Intro to LTSPICE Video RIT SPICE Models	Intro to LTSPICE.pdf Intro to LTSPICE.wmv MODELS.txt	Intro to LTSPICE	HW on Intro to LTSPICE
26.	MOSFET SPICE Models	SPICE MOSFET Models.pdf SPICE Parameter Calc.XLS	Intro SPICE_MOSFET_Models SPICE MOSFET Models	HW on SPICE Examples
27.	SPICE Examples More SPICE Examples	SPICE EXAMPLES.pdf More SPICE EXMPLES.pdf	SPICE Examples More SPICE Examples	HW on SPICE EXAMPLES
28.	Introduction to VLSI VLSI CAD	IntroVLSI.pdf VLSI-CAD.pdf		HW on Intro to VLSI
29.	Back End Processes	Back_End.pdf	Gas_Flow.wmv	
30.	Microcontrollers, DRAM and EEPROM	Microcontrollers.htm DRAM.pdf EEPROM.pdf	Arduino Sensor.wmv	

FACTORY TEAMS

Red Group	Orange Group	Yellow Group	Green Group	Blue Group
1.	1.	1.	1.	1.
2.	2.	2.	2.	2.
3.	3.	3.	3.	3.

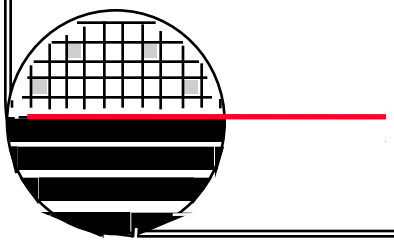
Every two weeks groups shift discipline (to the right). For example the red group does Diffusion week 1&2, Red does Lithography week 3&4, Red does CVD/Plasma week 5&6, etc.

Discipline

Diffusion	Lithography	PVD/Plasma Etch	CVD/PECVD	Wet Etch/CMP
Bruce Furnace	Canon Stepper	CVC601	ASM 6"LPCVD	Al Wet Etch
AG-RTP	SSI Track	Drytech Quad	P-5000	BOE Etch
Blue M Oven	CD Linewidth	Lam490	Nanospec	RCA Clean
Nanospec	Overlay	Lam4600	Spectromap	Hot Phos Nitride Etch
Spectromap	Branson Asher	Nanospec	Varian 350D	BOE
CDE Resistivity Map		Tencore P2		Solvent Strip
				CMP and CMP Clean
				Nanospec
				Surfscan
				SEM

While in each discipline the students will

- Process lots requiring steps in that discipline
- Perform follow up Inspection and Metrology
- Investigate and Update SPC data
- Monitor non-device process metrics
- Perform a "pass down" at the end of (2 weeks)
- Track lots in and out of Mesa

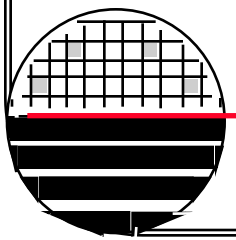


1-10-2013

MANUFACTURING IMPROVEMENT

If no factory lots are available in a specific discipline then group will do manufacturing improvement projects.

For Example:
BOE – Etch rate verification
RTP – Tool operation and recipe verification
PECVD – Tool operation and deposition rate verification,TEOS Oxide
Resist Coat Thickness Measurement using Spectromap for Coat.rcp and CoatMtl.rcp Recipes used by Factory
SPC Chart verification, evaluation and process capability improvement
Verify all MESA picture documents are correct
Verify MESA instructions are correct



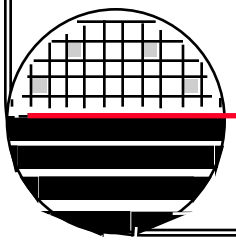
EXAMPLE PASSDOWN AT END OF ROTATION

Discipline: Lithography **Date:** Nov 30- Dec 9, 2013
Group Members: Matt McQuillan, Dave Pawlik

Lot Advancement:

F031013 – CC Photo –Changed Stepper Job to Align using TVPA Marks Only
added 2 µm shift to alignment key locations on pg 4/ in process file
F040119 – Resist Strip
F040614 – Active Photo
F031013 – LDDP Photo
F040920 – Resist Strip-Changed Stepper Job to Align using TVPA Marks Only
F040920 – P-Well Photo-Changed Stepper Job to Align using TVPA Marks Only
F030922- Resist Strip

Other: Short Loop Resist Coat Thickness measurement for Coat.rcp, Xpr=1.0 µm
Branson Asher often gives purge timeout error, select continue



TEXTBOOK/REFERENCES

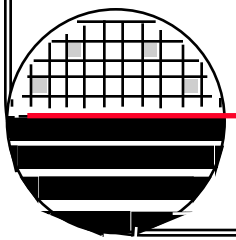
There is no required text for this course. You may wish to use the following textbooks as references. Lecture and Lab notes are available on Dr. Fuller's webpage:

1. Silicon Processing for the VLSI Era Volume I, S. Wolf and R.N. Tauber, Lattic Press, Sunset Beach, CA, 1986.

2. The Science and Engineering of Microelectronic Fabrication, S.A. Campbell, Oxford University Press, New York, NY, 1996.

3. VLSI Technology, Edited by S.M. Sze, McGraw-Hill Book Company, 1983.

4. Dr. Fuller's webpage: http://people.rit.edu/lffeee



HOMEWORK FORMAT GUIDLINES

1. At the top of the front page include the following information:

Rochester Institute of Technology **Your Name**
Microelectronic Engineering **Date**
MCEE 732 - Assignment Description

2. Name/date/page number on each page
3. Use 8.5”x11” paper with clean straight edges (no spiral notebook paper)
4. Leave room on the left margin for 3 hole punch.
5. Staple pages with one staple in top left at 45°.
6. Use black ink, avoid color because it will not copy well.
7. Type
8. Computer simulations must consist of a summary page followed by the hard copies of the data with key results underlined or boxed.
9. No cover or title.
10. Homework is due 1 week after finishing the module. Late homework will be graded but may have the grade lowered.

LABORATORY NOTEBOOK GUIDELINES

The laboratory Notebook is an important tool. Each student will be required to have such a notebook.

Name, Date, Description on Cover
Notebook will be of the permanently bound type
Include Multidisciplinary Teams, CMOS Process listings (3), Product Layouts (4), Operator Certification Sheet
Include Process Improvement Notes.
Number each page
Sign and Date each page (witness signature)
Use a diary type format to take notes of what you do each day. Include enough details so that a reader can follow what you did.
Tape printouts, data tapes, etc. correctly into the notebook.
Use ink.
Be neat.
See example notebook posted on Dr. Fuller's webpage