ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

EEEE 482 Electronics II

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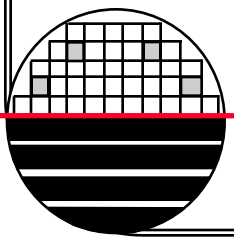

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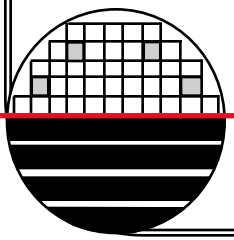


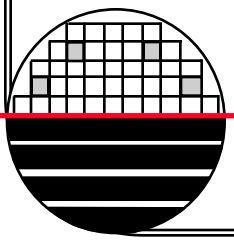
INTRODUCTION

This course will provide a continuation of electronic circuit design that was the topic of EEEE 481 Electronics I.

About half of the course will cover traditional topics on bipolar analog integrated circuits. The other half will cover traditional topics on digital integrated circuits.

This course will enhance the students understanding of MOSFET SPICE models used for todays submicron size devices

Finally, this course will be beneficial for students who would like to integrate CMOS and Bipolar electronic circuits with MEMS, creating Microsystems.



INSTRUCTOR INFORMATION

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TA Name:
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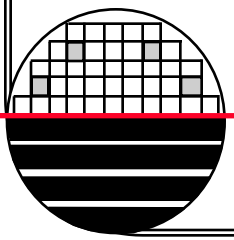


EEEE 482 COURSE DETAILS

EEEE 482 Electronics II

Prerequisites: EEEE 360 (Device Physics) or Equivalent
and EEEE 481 (Electronics I)

Course Goals: This is the second course in a two course sequence in electronic circuit design. The course will cover BJT and MOS electronic analog and digital circuit design.

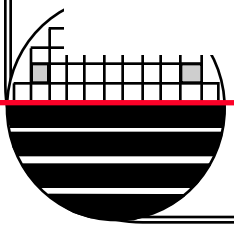
Format: The lecture meets four times per week and the lab meets one time per week.

Laboratory: Monday 8:00am, Monday 2:00pm and Wednesday 11:00am
Room 09-3200, 09-3280 and 09-3280

Meeting Days: T, W, R, F
Time: 2:00 pm
Lecture Room: INS-1140

Grade:

Homework	25%
Exams and Quizzes	25%
Laboratory	25%
Final Exam	25%



EEEE 482 LECTURE SCHEDULE

Rochester Institute of Technology
Electrical and Microelectronic Engineering
Dr. Lynn Fuller

Revised: August 15, 2014

EEEE 482 Electronics II

Lesson No.	Discussion Topic	Document	
1.	Getting Organized, Course Outline, Diode Review	out_EEEE482.pdf Diode_Review.pdf	
2.	Diode Review	Diode_Review.pdf pn_electrostatics_current_temp.xls	
3.	BJT Basics	BJT Basics.pdf	
4.	BJT Amplifiers	BJT_Amplifiers.pdf	
	Week 1 Lab Introduction		
5.	BJT Amplifiers	BJT_Amplifiers.pdf	
6.	BJT Amplifiers	BJT_Amplifiers.pdf	
7.	BJT Amplifier Examples	CE-BJT-Simple.XLS CE-BJT-Analysis.XLS CE-BJT-Design.XLS	
8.	Multistage BJT Amplifiers	BJT_Amplifiers.pdf	
	Week 2 Lab SPICE Review		
9.	Multistage BJT Amplifiers	BJT_Amplifiers.pdf	
10.	Design Example		
11.	Summary and Review		
12.	BJT IC Design - Differential Amplifier	BJT IC Design.pdf	

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12.	BJT IC Design - Differential Amplifier	BJT IC Design.pdf	
	Week 3 Lab Semiconductor Device Parametric Testing		
13.	Exam 1		
14.	BJT IC Design - Differential Amplifier	BJT IC Design.pdf	
15.	BJT IC Design - Current Sources	BJT IC Design.pdf	
16.	BJT IC Design - Output Stages	BJT IC Design.pdf	
	Week 4 Lab CE Amplifier Design		
17.	Go Over Exam 1 and Power Conditioning	Power_Conditioning.pdf	
18.	Basic Analog Circuits	Basic Analog Circuits.pdf	
19.	Frequency Response of Electronic Circuits	Frequency_Response.pdf	
20.	Frequency Response of Electronic Circuits	Frequency_Response.pdf	
	Week 5 Lab Differential Amplifier		
21.	Frequency Response of Electronic Circuits	Frequency_Response.pdf	
22.	Frequency Response of Electronic Circuits	Frequency_Response.pdf CE-BJT-Analysis-DC-AC-Freq.XLS	
23.	Filters, Network Analyzer	Selected_Filter_Circuits.pdf	
24.	Feedback	Feedback.pdf	
	Week 6 Lab Multistage Amplifier Design		
25.	Feedback	Feedback.pdf	
26.	Feedback	Feedback.pdf	
27.	Feedback and Stability	Feedback.pdf	
28.	Summary and Review		
	Week 7 Lab Global Feedback		

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29.	Exam 2		
31.	Advanced MOSFET Basics	MOSFET_Basics.pdf	
32.	Submicron MOSFET Models	SPICE_MOSFET_Models.pdf	
32.	Introduction to Digital Electronics	IntroVLSI.pdf	
	Week 8 Lab - Catch Up		
33.	Go Over Exam 2 and AtoD and DtoA Conversion	AtoD and DtoA Conversion_Circuits.pdf	
34.	Voltage Transfer Curve (VTC)		
35.	RTL and Other Inverter Logic Families		
36.	NMOS Inverters and Logic		
	Week 9 Lab MOSFET SPICE Models		
37.	CMOS Inverters and Logic		
38.	CMOS Combinational Logic		
39.	CMOS VLSI Design		
40.	CMOS Sequential Logic		
	Week 10 Lab NMOS Inverters		
41.	Power, delay		
42.	Interconnect R & C		
43.	Propagation delay		
44.	Propagation delay		
	Week 11 Lab CMOS Inverters		
45.	Exam 3		

EEEE 482 LECTURE SCHEDULE

46.	Path delay		
47.	Transmission gates		
48.	Dynamic logic, domino logic		
	Week 12 Lab CMOS Sequential Logic		
49.	Semiconductor Memory, Decoders, Sense Amplifiers		
50.	SRAM		
51.	DRAM	DRAM.pdf	
52.	EEPROM	EEPROM.pdf	
	Week 13 Lab Propagation Delay		
53.	Flash Nand and Nor		
54.	Memory Special Topics		
55.	Charge-pump		
56.	RLC		
	Week 14 Lab MOS Based Memory		
57.	Energy Harvesting	Energy Harvesting.pdf	
58.	Single Supply Op Amp Circuits	OpAmpSingleSupply.pdf	
59.	PCB Design, Fabrication and Surface Mount	RIT_Package.pdf Surfacemount.pdf	
60.	Microcontrollers	Microcontrollers.htm	
	Week 15 No Lab		
61.	Final Exam		

TEXTBOOK/REFERENCES

There is no required text for this course. You may wish to use the following textbooks as references. Lecture and Lab notes will be provided.

1. Microelectronic Circuits, Fifth (or Sixth) Edition, Adel Sedra and Kenneth Smith, Oxford University Press, 2001.

2. Analysis and Design of Digital Integrated Circuits, David Hodges, Horace Jackson and Resve Saleh

3. Any Device Physics textbook.

4. PSPICE Users Guide.

5. Microchip Manufacturing, S. Wolf, Lattice Press, Sunset Beach, CA, 2004.

HOMEWORK FORMAT GUIDLINES

1. At the top of the front page include the following information:

Rochester Institute of Technology **Your Name**
Microelectronic Engineering **Date**
EEEE 482- Assignment Description

2. Name/date/page number on each page
3. Use 8.5”x11” paper with clean straight edges (no spiral notebook paper)
4. Leave room on the left margin for 3 hole punch.
5. Staple pages with one staple in top left at 45°.
6. Use black ink, avoid color because it will not copy well.
7. Type
8. Computer simulations must consist of a summary page followed by the hard copies of the data with key results underlined or boxed.
9. Covers and title pages should feed through the copier also.
10. Homework is due 1 week after finishing the module. Late homework will be graded but may have the grade lowered.

EEEE 482 LABORATORY DETAILS

EEEE 482 Electronics II Laboratory

Prerequisites: EEEE 360 (Device Physics) or Equivalent
and EEEE 481 (Electronics I)

Course Goals: This is the second course in a two course sequence in electronic circuit design. The course will cover BJT and MOS analog and digital electronic circuit design.

Format: The lecture meets three times per week and the lab meets one time per week.

Laboratory:		
	8:00am to 10:50am Monday	GLE-3200
	2:00pm to 4:50pm Monday	GLE-3280
	11:00pm to 2:00pm Wednesday	GLE-3280

Laboratory Grade:		
	Pre-lab	10%
	Simulations	10%
	Lab Performance	10%
	Each Tech Memo	10%

ACCESS LAB DOCUMENTS FROM DR. FULLERS WEBPAGE

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Revised: August 14, 2014

EEEE 482 Electronics II Laboratory

Week No.	Topic	Document	References	Assignment
1.	Introduction, Schedule, Policies, Tech Memo Template	EEEE 482 Lab Outline.pdf Tech Memo Instructions.doc		Read These Documents
2.	SPICE Review LT SPICE is very similar to OrCAD PSPICE. It is free, has no limits on number of components and easy to use. Ideal for your personal computer.	OrCAD PSPICE Intro OrCAD PSPICE Intro.pdf OrCAD PSPICE Models.txt	Intro to LTSPICE LTSPICE Models.txt Intro to LTSPICE.wmv	Review LTSPICE Do SPICE Intro Examples
3.	Semiconductor Device Characteristics and Parametric Testing	BJT Characterization.pdf		Do BJT Characterization HW
4.	Common Emitter Amplifier Design	BJT Amplifiers.pdf EEEE 482 Lab0 Rev2 1.pdf		No Report
5.	Differential Amplifier with Resistive Load and Current Source Bias	EEEE 482 Lab1 Rev2 3.doc		Tech Memo Due Next Week
6.	Multistage Amplifier Design	EEEE 482 Lab2 Rev2 0.doc		Tech Memo Due Next Week
7.	Global Feedback in BJT Multistage Amplifier	EEEE 482 Lab3 Rev1 3.doc		Tech Memo Due Next Week
8.	This week will be used to get caught up ... finish up all the BJT labs.			
9.	Review of SPICE MOSFET Models Work on your Prelab for NMOS Inverters (Long Prelab)	Intro SPICE MOSFET Models	Intro SPICE MOSFET Models SPICE MOSFET Models RIT_Models_For_LTSPICE.txt	Review these documents
10.	Design, Simulation and Testing of NMOS Inverters	EEEE 482 Lab4 Rev2 6.doc		Tech Memo Due Next Week
11.	CMOS Inverter and CMOS Combinatorial Logic	EEEE 482 Lab5 Rev2 7.doc		Tech Memo Due Next Week
12.	CMOS Sequential Logic	EEEE 482 Lab6 Rev2 5.doc		Tech Memo Due Next Week
13.	Propagation Delay Through CMOS Logic	EEEE 482 Lab7 Rev2 4.doc		Tech Memo Due Next Week
14.	MOS Based Memory	EEEE 482 Lab8 Rev2 3.doc		Tech Memo Due Next Week
15.	No Lab			

LABORATORY SUPPLIES

Prototype board
Breadboard supplies – wires, pliers, wire stripper
Scope Probes
Tape, scissors